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Low-Power and High-Speed Tri-State Inverter Structures and its application

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Abstract: In digital integrated circuit applications, the standard CMOS logic based tri-state inverter lies in the critical path that affects the overall speed of the system. The internal circuitry in tri-state inverter is responsible for the large time-delay and huge power. Whereas the C^2MOS logic tri-state inverter is operated at higher speeds, but dissipates more amount of power due to precharge of pMOS transistor per each clock cycle. To overcome the problems, three tri-state inverter structures have been proposed. The three structures i.e. Transmission gate (TG) based tri-state inverter, pseudo-nMOS with active enable pull-up tri-state inverter and Pass Transistor (PT) based tri-state inverter are designed and examined using PSPICE and the model parameters of a 0.13 µm CMOS technology. The proposed tri-state inverter structures are compared with existing ones exhibits better delay performance and energy consumption. Due to reduced transistor count and usage of Euler path approach, optimization of an area takes place by the PT based tri-state inverter by a factor of about 79.49% and 50% as compared to standard CMOS and C^2MOS logic based tri-state inverters.

Keywords: Low-voltage low-power logic styles, Tri-state inverter, Static decoders, performance comparison.

I. INTRODUCTION

Mostly tri-state inverters are preferred in digital integrated circuits to permit connectivity of the multiple devices on a single bus without any loss of information. Processors, memory architectures, programmable logic devices and decoders are some examples of the system involving them. Tri-state inverters are classified into two types: active enable high tri-state inverter and active enable low tri-state inverter [1, 2].

The explanation for the existing topologies for the tri-state inverter structures is as follows,

1. The standard tri-state buffer followed by an inverter consists of 1 NAND gate, 1 NOR gate and 3 NOT gates, when designed with respect to CMOS logic it needs 14 transistors. The main advantage of static CMOS logic is its robustness against to device variations, voltage scaling, easy to design, low-power and layout is straight forward with regular structure and supported by CAD tools to a great extent. But a major amount of delay and power is contributed by the tri-state inverter. Because it requires more number of transistors to implement which occupies large chip area and higher operating speed is not possible due to large input capacitance i.e. parasitic delay and logical effort [1].

2. The conventional C^2MOS tri-state inverter [2] [3] [4] consists of 6 MOSFET transistors designed with respect to C^2MOS logic. The advantages dynamic C^2MOS logic over standard CMOS logic circuits: 1. Occupies small area due to less number of transistors. 2. The parasitic capacitance of the circuit is small, so that higher operating speeds are possible. 3. The dynamic circuits operate under clock signal require careful clocking, consume more dynamic power. The circuit is sensitive to noise whenever the clock signal is operating in evaluation phase. Charge distribution is a major problem in the circuit design and must be considered [5].

In this paper, we presented three tri-state inverter structures using TG based tri-state inverter, pseudo-nMOS with active enable pull-up tri-state inverter and PT based tri-state inverter. The proposed tri-state inverter structures require less number of transistor counts and operate at higher speeds with less energy consumption. The remaining part of the paper is organized as follows. Section 2 describes the design and implementation of tri-state inverter structures. Section 3 explains the simulation results and performance comparison. An application i.e. 2-to-4 decoder related to tri-state inverter is simulated in section 4 and section 5 ended up with a conclusion.

II. PROPOSED TRI-STATE INVERTER STRUCTURES

A. *Transmission gate (TG) based Tri-state Inverter*

The Figure1 shows the tri-state inverter designed with respect to TG logic requires 6 transistors. The parallel connection of two pass transistors i.e. M3 and M4 realize TG

logic provides a better driving capability. Here EN denotes the enable as active high input signal connected to the gate terminal of M4 transistor and its complement is connected to the gate terminal of M3 transistor. The signal A is the input connected to the source terminals of M3 and M4 transistors, drain terminals are shorted together and connected to the input of CMOS inverter (M5 and M6) as shown in Figure1. The operation of the proposed TG based tri-state inverter is shown in Table1. The TG logic requires lower transistor count as compare to CMOS tri-state inverter which reduces the critical path delay and occupies less silicon area on the chip.

Table1. Functional table

EN	A	M1	M2	M3	M4	M5	M6	OUT
1	1	OFF	ON	ON	ON	OFF	ON	0
1	0	OFF	ON	ON	ON	ON	OFF	1
0	1	ON	OFF	OFF	OFF	OFF	OFF	Z
0	0	ON	OFF	OFF	OFF	OFF	OFF	Z

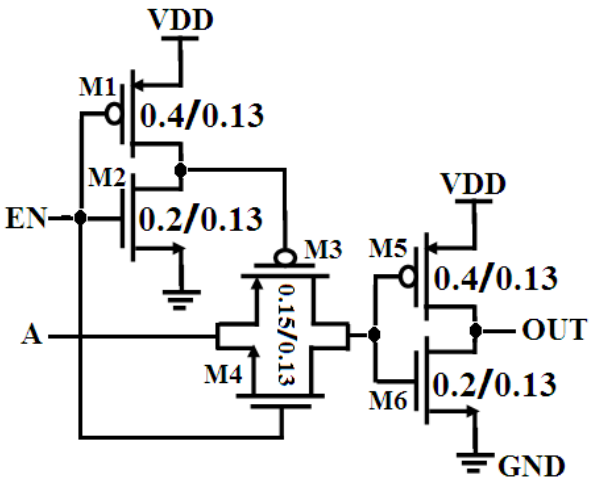


Figure1. Proposed tri-state inverter circuit using TG logic.

B. *Pseudo-nMOS with active enable pull-up tri-state inverter*

The Figure2 shows the tri-state inverter designed with respect to pseudo-nMOS logic with active enabled pull-up requires 4 transistors. The series connection of two transistors i.e. M3 and M4 realize pseudo-nMOS logic, whereas the M3 transistor's gate terminal connected to the ground is replaced by pseudo-nMOS gate with active enable pull-up as shown in Figure2. The EN denotes enable as active high input signal connected to the gate terminal of M3 transistor using a CMOS inverter (M1 and M2). The input signal A is connected to the gate terminal of M4 transistor. The operation of the pseudo-nMOS based tri-state inverter is shown in Table2. It requires lower transistor count as compare to CMOS tri-state inverter and C^2MOS tri-state inverter which reduces the critical path delay and occupies less silicon area on the chip.

Table2. Functional table

EN	A	M1	M2	M3	M4	OUT
1	1	OFF	ON	ON	ON	0
1	0	OFF	ON	ON	OFF	1
0	1	ON	OFF	OFF	ON	Z
0	0	ON	OFF	OFF	OFF	Z

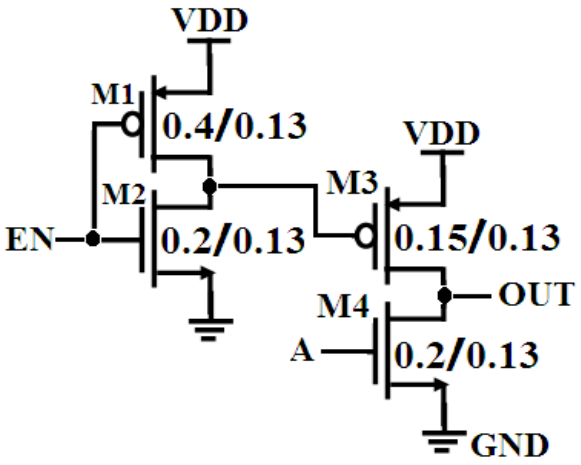


Figure2. Proposed tri-state inverter circuit using pseudo-nMOS logic.

C. *Pass Transistor (PT) based tri-state inverter*

The Figure3 shows the tri-state inverter designed with respect to pass transistor logic requires 3 transistors.

Table3. Functional table

EN	A	M1	M2	M3	OUT
1	1	OFF	ON	ON	0
1	0	ON	OFF	ON	1
0	1	OFF	OFF	OFF	Z
0	0	OFF	OFF	OFF	Z

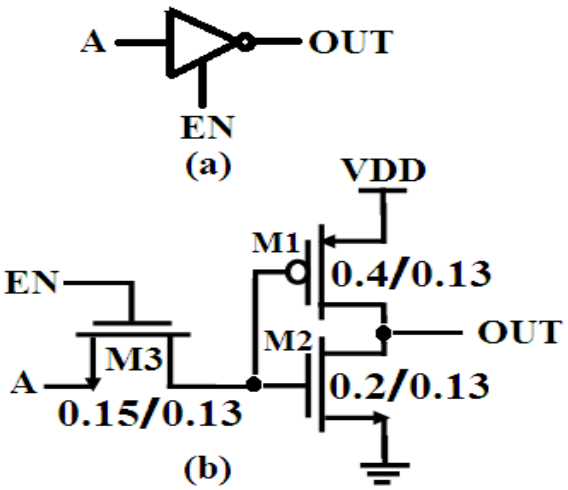


Figure3. (a) tri-state inverter logic symbol (b) Proposed tri-state inverter circuit using PT logic.

Here M3 is the pass transistor and transistors M1 and M2 forms a CMOS inverter. The input signal A is connected to the source terminal and the EN input signal connected to the gate terminal of the pass transistor. The drain terminal of M3 transistor is connected to the input of the CMOS inverter. The operation of the PT based tri-state inverter is shown in Table3. It requires lower transistor count as compare to existing tri-state inverters which reduces the critical path delay and occupies less silicon area on the chip.

Table4. Comparison of design metrics of the different tri-state inverters

Tri-state Enable active-high Inverters	Logical effort (G)	Parasitic delay (P)	Transistor count	Area (μm^2)	Minimum VDD	Performance parameters at supply voltage VDD = 1V		
						Delay (Psec)	Dynamic Power (µW)	Power delay product (fJ)
Static CMOS	6.15	1.53	14	5.12	0.3	257	394	101.25
Clocked CMOS	3.07	1.53	06	2.10	0.34	192	242	46.45
TG Logic	1.53	1.53	06	1.98	0.32	175	214	37.14
Pseudo-nMOS	2.04	0.89	04	1.15	0.33	154	184	28.33
Pass Transistor	0.76	1.53	03	1.05	0.35	126	158	20.02

III. SIMULATION RESULTS AND COMPARISONS

The proposed tri-state inverter structures are simulated using pyxis schematic of mentor graphics tool at 0.13µm technology. The simulated waveform of the existing and proposed tri-state inverter circuits is shown in Figure4. In this section, the proposed tri-state inverter circuits are compared with existing ones by varying the supply voltage in the range of 0.4 - 1V at 0.13 µm technology. The minimum V_{DD} required for operating the various tri-state inverter circuits is shown in Table4.

The graph shown in Figure5 (a) denotes the propagation delay verses supply voltage. The proposed tri-state inverter circuits occupy less delay for all considered supply voltages. The delay of the proposed tri-state inverter circuits is minimized due to optimization of the internal circuitry in tri-state inverter, responsible for the large time-delay and huge power and reduced transistor count. The optimization of transistor count leads to the reduction of logical effort (G) and parasitic delay (p) of the circuit [6]. The calculated theoretical value of G, p is shown in Table4.

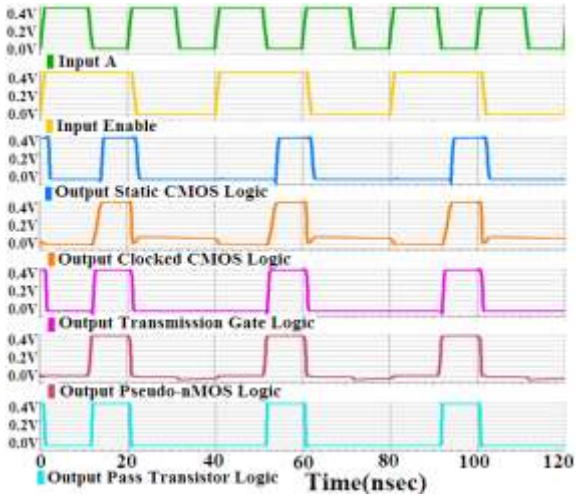
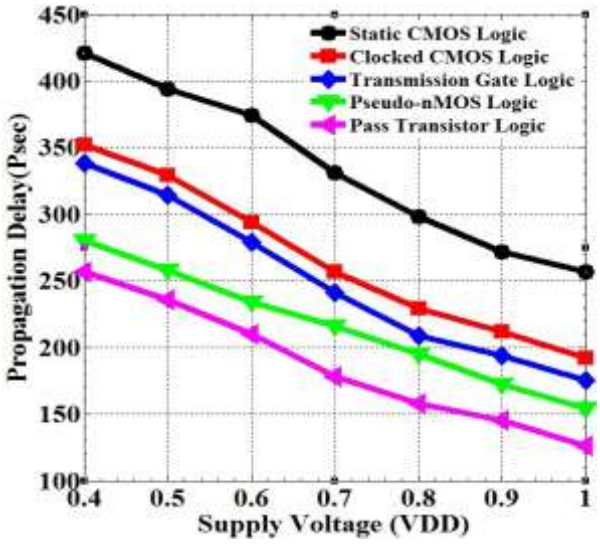
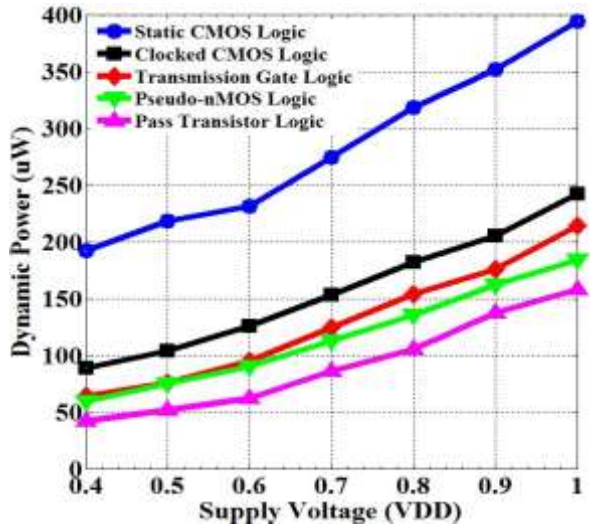


Figure4. Simulated waveform of the available and proposed tri-state inverters.



(a)



(b)

Figure5. (a) Propagation delay vs. supply voltage (b) dynamic power vs. supply voltage of different tri-state inverters.

The graph shown in Figure5 (b) denotes the dynamic power verses supply voltage. The proposed tri-state inverter circuits

occupy less dynamic power for all considered supply voltages. The total capacitance i.e. C_{TOTAL} of the circuit depends on the input capacitance, switching, load capacitance (C_L). Due to reduced transistor count, minimization of capacitance takes place which is directly proportional to the dynamic power [6] as given by equation (1). Where V_{DD} is the supply voltage, V_t is the threshold voltage, f is the operating frequency, W is the width of the transistor and L is the channel length of the transistor. The maximum and minimum power delay product obtained by the static CMOS logic and PT logic tri-state inverter circuits as shown in Figure6.

$$p = C_L V_{DD}^2 f = WL C_{ox} V_{DD}^2 f \qquad (1)$$

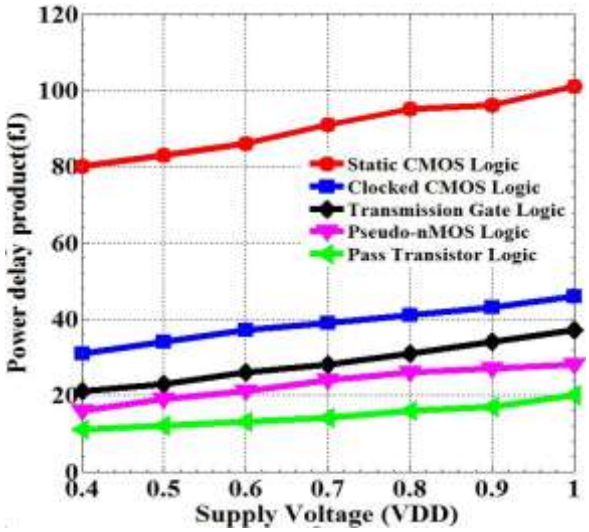


Figure6. Power delay product vs. supply voltage of different tri-state inverters.

A. *Aspect ratios of the transistor*

The power and delay of the circuit is inversely proportional to each other. In order to reduce the delay of the circuit, the aspect ratios of the transistor is increased by a factor of two which would increase the switching speed of the circuit. Increase of Width-to-Length ratios will increase the gate capacitance, load capacitance and area of the circuit leads to dynamic power dissipation [7]. To keep the tri-state inverter area within the reasonable value and to attain better performance of the tri-state inverter circuit, maintain the sizes of all the transistors for the proposed tri-state inverters and standard tri-state inverters are given by

$$\left(W/L\right)_{pMOS} = 0.4\mu m / 0.13\mu m$$

$$\left(W/L\right)_{nMOS} = 0.2\mu m / 0.13\mu m$$

For this purpose BSIM3 LEVEL 53 nMOS. 1 model and pMOS. 1 model transistors with V_{Tn} = 0.31 V and V_{Tp} = -0.29 V are used.

B. *Comparison of area*

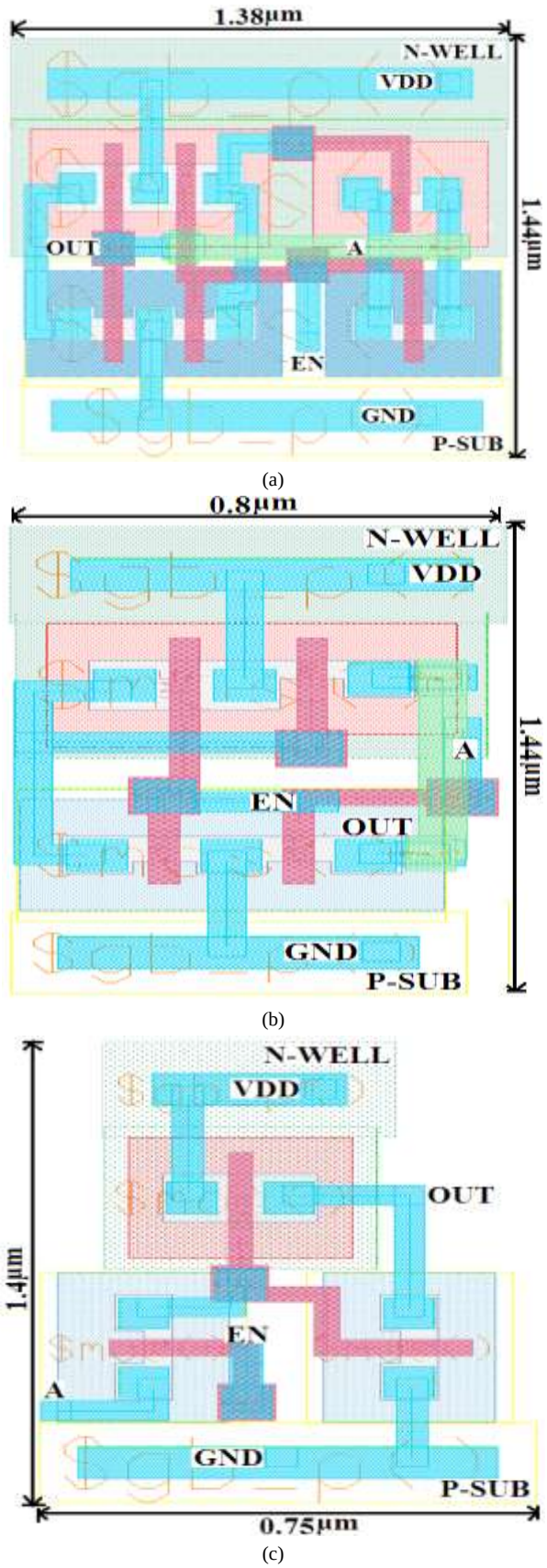


Figure7. Proposed tri-state inverter layout using (a) TG logic (b) Pseudo-nMOS with active enable pull-up (c) PT logic.

The layout of the proposed tri-state inverter structures is shown in Figure7 using mentor graphics IC layout 0.13 µm CMOS technology design rules. Because of the space constraint the layout of the other tri-state inverters are not shown. But the numerical value of the area occupied by the tri-state inverter circuits is shown in Table4. When compare to standard CMOS and C^2MOS tri-state inverters, the proposed ones occupy less amount of silicon area on the chip due to reduced transistor count as shown in Table4. By using Euler's path approach [8], optimization of an area takes place by the PT logic based tri-state inverter by a factor of about 79.49% and 50% as compared to standard CMOS and C^2MOS tri-state inverters.

Table5. Comparison of design metrics of the different tri-state inverters for 2-to-4 static decoder circuit

Tri-state active-high Enable Inverters	Logical effort (G)	Parasitic delay (P)	Transistor count	Area (μm^2)	Minimum VDD	Performance parameters at supply voltage VDD = 1V		
						Delay (Psec)	Dynamic Power (µW)	Power delay product (aJ)
Static CMOS	11.07	5.22	42	13.64	0.3	407	408	166.05
Clocked CMOS	7.99	5.22	34	10.62	0.34	342	256	87.55
TG Logic	6.45	5.22	34	10.5	0.32	325	228	74.1
Pseudo-nMOS	6.96	4.58	32	9.67	0.33	304	198	60.19
Pass Transistor	5.68	5.22	31	9.57	0.35	276	172	47.47

IV. IMPLEMENTATION OF 2-TO-4 DECODER USING TRI-STATE INVERTER CIRCUITS

In the architecture of memories, decoder plays an important role by selecting a particular memory cell in the array with a given specific address by enabling the word-line and bit-lines. Decoders are classified into two types: static decoder and dynamic decoder. Usually static CMOS logic styles are used in the decoding process of a SRAM [9].

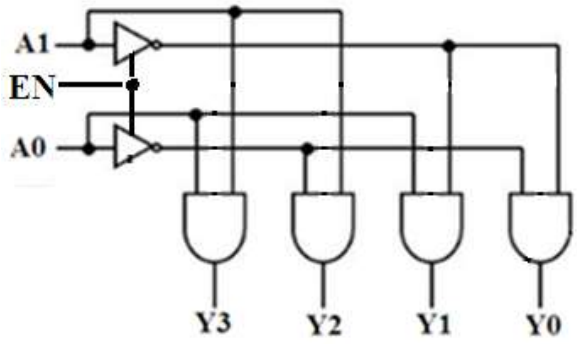


Figure8. Schematic diagram of a 2-to-4 static decoder.

Table6. Truth table of a 2-to-4 static decoder

	Inputs		Outputs			
EN	A0	A1	Y3	Y2	Y2	Y0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

In the architecture of SRAM, tri-state inverters are used as address buffers in the row/column decoding section and to transfer the date in to the memory and out of the memory tri-state buffers are used. The schematic circuit diagram and truth table of the 2-to-4 static decoder is shown in Figure8 and Table6 [1] [9]. The simulation results and performance parameters of the 2-to 4 static decoder using different tri-state inverters is shown in Table5. The implementation of 2-to-4 decoder using proposed tri-state inverter structures as address inputs having better delay performance and less energy consumption due to reduced critical path and transistor count.

V. CONCLUSION

This paper presents three tri-state inverter circuits using TG logic, pseudo-nMOS with active enable pull-up logic PT logic. The critical path produced due to the internal circuitry of the tri-state inverter reduces both the size and count of the transistors. With this, the logical effort, parasitic delay and C_{TOTAL} of the tri-state inverter are minimized, which exhibits better delay and energy performance. An optimization of an area takes place using Euler's path approach by the PT logic based tri-state inverter by a factor of about 79.49% and 50% as compared to standard CMOS and C^2MOS tri-state inverters. For high performance, low-power and high-density memory architectures used in mobile and storage applications, the essential benefits of the proposed tri-state inverters could be fully utilized.

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REFERENCES

[1] John F. Wakerly, "Digital Design Principles and Practices", 4th edition, United States, Pearson Education, India, chapter 3, pp. 128-129, ISBN: 9780131733497, 2006.

[2] Neeta Pandey, Bharat Choudhary, "Improved tri-state buffer in MOS current mode logic and its application", Analog Integrated Circuits and Signal Processing, Vol. 84, No. 2, pp. 333-340, 2015.

[3] M. Alioto, G. Di Cataldo, and G. Palumbo, "Optimized design of high fan-in multiplexers using tri-state buffers", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Vol. 49, No. 10, pp. 1500-1505, 2002.

[4] Bae, Woorham, et al, "A 7.6 mW, 414 fs RMS-jitter 10 GHz phase-locked loop for a 40 Gb/s serial link transmitter based on a two-stage ring oscillator in 65 nm CMOS", IEEE Journal of Solid-State Circuits, Vol. 51, No. 10, pp. 2357-2367, 2016.

[5] Kamran Eshraghian, Douglas A. Pucknell and Sholeh Eshraghian, "Essentials of VLSI circuits and systems", Prentice-Hall of India, chapter 6, pp. 149-150, ISBN: 9788120327726, 2005.

[6] Neil H. E. Weste, David Harris and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd ed., chapter 4, pp. 118-123, United States, Pearson Education India, ISBN: 9780321149015, 2005.

[7] Venkata Rao Tirumalasetty, Srinivasulu Avireni, "Modified level restorers using current sink and current source inverter structures for BBL-PT full adder", Radioengineering, Vol. 21, No. 4, pp. 1279-1286, 2012.

[8] Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits", 3rd ed., chapter 7, pp. 297-299, Tata McGraw-Hill Education, New York, ISBN: 9780070530775, 2003.

[9] Kiat-Seng Yeo, Kaushik Roy, "Low voltage, low power VLSI subsystems", 1st ed., chapter 6, pp. 193-198, McGraw-Hill, Inc., New York, ISBN: 9780070677500, 2009.

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