International Journal of Modern Electronics and Communication Engineering (IJMECE) ISSN: 2321-2152
Volume No 4, Issue No 6, November, 2016

FPGA based Efficient Digital Signal generator

Mrs. K. Lakshmi[1]
Department of ECE
Vignan's Institute of Information Technology
Visakhapatnam, India
E-mail: kadalilakshmi@gmail.com

Dr. A Naga Jyothi[2]
Department of ECE
Vignan's Institute of Information Technology
Visakhapatnam, India
E-mail: aggala.jyothi@gmail.com

Mrs S. Pushpalatha[3]
Department of ECE
Vignan's Institute of Information Technology
Visakhapatnam, India
E-mail: suggu.pushpa@gmail.com

Abstract: This paper describes a technique that utilizes the memory very efficiently for the successful generation of periodic waveforms in their digital format and illustrates its implementation in Field Programmable Gate Array (FPGA) technology. Digital waveforms such as sinusoidal, trapezoidal, square wave, triangular wave and addition of two waveforms are generated using efficient look up table method to reduce the hardware implementation using Very High Speed Integrated Circuit hardware Description Language (VHDL) and FPGA. The proposed design has been simulated and validated using ModelSim software and implemented using Xilinx Vitex-6 FPGA and verified using Xilinx On-Chip Debugging tool Chip scope-pro software. The implemented results shows that any periodic function can be realized directly in digital form without need of analog to Analog to Digital Converter using FPGA.

Keywords: FPGA, VHDL, Signal generator; ChipScope pro.

I. INTRODUCTION

Generations of periodic waveforms in all commercial and military applications are necessary and should be implemented effectively to reduce the hardware and complexity. Signal generators are used in wide range of applications including communications design and test, pulse generation, high speed low-jitter data and clock source and mixed-signal design and test, biomedical applications [1].

Communication and digital signal processing applications of today are often developed as fully integrated systems on one single chip and are implemented as application specific integrated circuits using e.g. VLSI technology.

As the systems are getting more and more complex, in terms of speed and performance, the chip size and the design time tend to increase rapidly. This will result in search for cheaper and less time consuming alternatives.

One alternative is field programmable gate arrays, so called FPGAs. The FPGAs are getting faster, cheaper and the number of gates increases all the time. A long list of ready-to-use functional blocks, so called intellectual property (IP) blocks, can be used in FPGAs.

The latest FPGAs can also be bought with one or more embedded processors, in form of hard processor cores or as licenses for soft processor cores. This will speed up the design phase and of course also decrease the crucial time to market even more.

The rest of the paper is organized as follows. In Section 2, FPGA architecture is discussed in brief. Implementation details are then discussed in section 3. In section 4 simulation results using model Sim and FPGA implementation and test results are discussed. The final section completes the paper with some conclusions.

II. BLOCK DIAGRAM

The block diagram of FPGA efficient signal generator is shown in the figure.1. It consists of major three components. One is clock generator which is used to implement the frequency of the generated signal. There is a provision to select and vary the generated signals based on the requirement. The output of FPGA will be digital and this digital data is given to Digital-to-Analog Convertor (DAC). DAC converts the digitally created signal to analog form thus creating a versatile, flexible signal generator. The DAC and FPGA share a single clock source to avoid clock jitters and mismatches. Since we are using FPGA as a hardware part, in future easily upgrade the signal generator by altering the FPGA design.

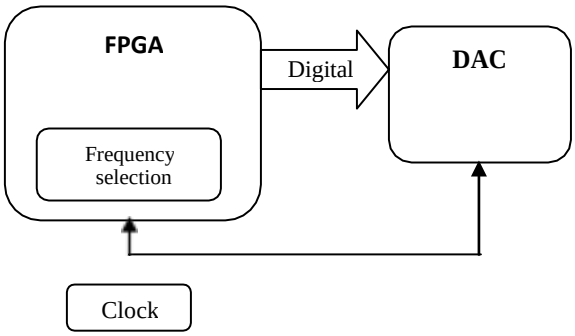

Figure1. Block diagram of proposed system.

This method uses the phase accumulator which is nothing but a counter that resets periodically after n clock pulses based on the frequency selection. Hence the period of the waveform is decided by the frequency of the signal to be selected by the frequency module. By using phase accumulator, it converts the phase value into digital value that represents the amplitude of the signal. Different signals are generated by converting the digital values into corresponding amplitude values by using digital to analog converter.

Digital to Analog Converter:

Very high performance and high frequency DAC chipDAC3283 from Texas Instruments which could provide 800Mspssampling rate, 16 bits resolution with an 8-bit LVDS input data bus with on-chip termination [6]. This chip uses LVDS logic standard for data interface. The functional block of DAC3283is as shown in Figure.2.The output of DAC chip is a differential current signal and its second harmonic signal will be filtered by a RF transformer. The differential current signal will be transformed to a single end current signal and its high frequency part will be filtered through an appropriate bandwidth low-pass filter. According to the needs current voltage conversion and signal amplification will be processed for generating a stable, low noise analog waveform.

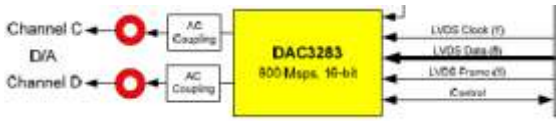

Figure2. Block diagram of proposed system.

III. IMPLEMENTATION

The following figure.3 shows the FPGA modules to implement the signal generators [5]. This design has been implemented in VHDL language and complete design has been verified in Model-Sim software and system is implemented in Virtex-6 development board [4]. The major inputs for the FPGA is clock which is a crystal clock source of 66MHz, reset input which is used to reset the board with power on and selection lines those are digital IO lines in FPGA are configured as input and normally high and becomes low when these are lines are made on by switch. The system clock of 66 MHz is interfaced to the FPGA and based on the clock period, all modules are implemented and functioned. In FPGA, there is a possibility to upgrade the clock frequency by using Digital phase locked loops there by clock frequency can be increased and it can be used for the reference clock[2]. On the other way, the same clock can be downgraded to generate the signals of less frequency than the clock source. Frequency selection module is designed to implement various the signal frequencies.

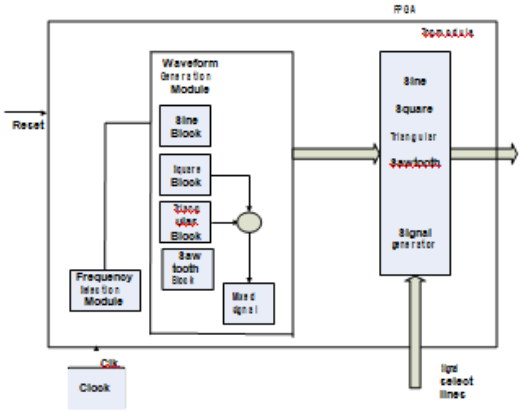

Figure3. FPGA Modules Implemented

The generated reference clock is given to the waveform generator module which samples the waveform data memory and drive the D/A converter. When a waveform is needed to be generated, the software will calculate sampling points and store them in the waveform memory. The outputs of phase accumulator under the control of the reference clock are used as the address of the waveform memory. The phase accumulator is an N bits counter, and W is the high W bits of the N bits. It is equivalent to a sampling output of the waveform data when the phase accumulator operated once. And the accumulated value is the frequency control word which controls the frequency of the outputted waveform. Then the waveform is generated after the D/A converter and the filter. Different signals are generated like sine wave, square wave, triangular wave, saw-tooth wave and addition of above two signals. The method employed to generate the signals is lookup table method in which all sine values a for required samples are generated and store in a memory and uses symmetric property of sine wave and the memory requirement using this method is very less and more flexible to change the resolution of the digital data. This method yields very less error compared to other methods and the hardware realization is also

simple. Finally the output of the signal generator module is given to the signal selection module which is used to select the signal based on the input selection lines. There inputs are employed here to select the eight combinations of signal sources. The module is nothing but a multiplexer which directs the desired signal source to output based on the selection lines.

IV. RESULTS

The signal generator modules are implemented in VHDL language and simulation studies has been carried out and verified using Model-Sim software. VHDL test bench is used to generate test vectors for Unit under Test for simulation purpose. The simulation results for all modules are explained below. The complete design has been verified and system is implemented in Virtex-6 development board and on-chip debugging is performed using Xilinx ChipScope-pro debugging tool [3].Different signals in digital form are generated using FPGA and the output in digital form is given to DAC to generate the signals in analog form. The following figure.4shows the simulated and verified waveform of 16-bit digital square wave and digital saw-tooth wave for selection lines (000) and (001) respectively.

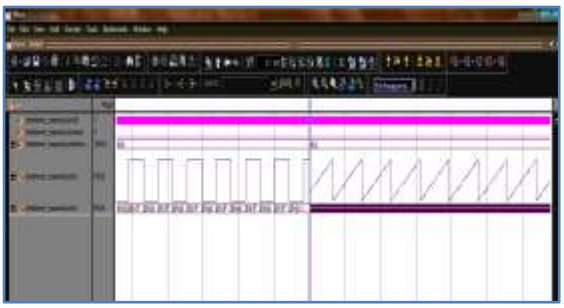

Figure4. Simulated results using Model-Sim

The following figure.5 shows the simulated and verified waveform of 16-bit digital triangular wave and digital sine wave for selection lines (010) and (011) respectively.

Figure5. Simulated results using Model-sim

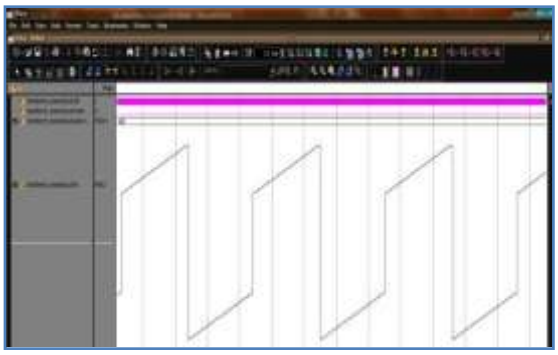

Figure6. Simulated results using Model-Sim

The figure.6 shows the simulated and verified waveform of 16-bit digital waveform for addition of square wave and saw-tooth wave for selection lines (100).

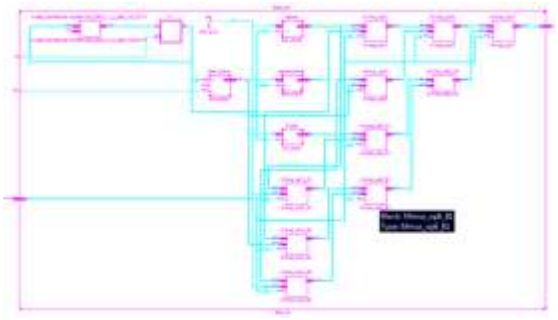

Figure7. RTL schematic of FPGA design.

The VHDL design of the signal generator is implemented on the virtex-6 FPGA with Digital to Analog converter board. The test results show that the desired signals of various frequencies are successfully achieved. The figure.6 shows the RTL schematic of the design which is implemented on FPGA. The hardware and test setup is shown in the figure.

Figure8. Hardware and Test setup of the system.

Three DIP switches in the board are configured as selection lines and desired signals are generated by FPGA in digital form and it is given to the Digital to Analog Converter which gives the signals in analog form.

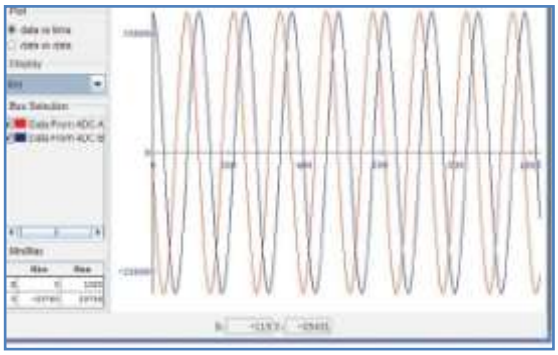

Figure.9: single ended output of sine waveform

The above figure shows the single ended sine waveform output from digital to analog converter.

V. CONCLUSION

This paper introduces a FPGA based efficient signal generator that requires very less hardware, less memory and it is faster than other methods. The system is implemented, simulated and designed on virtex-6 FPGA board. This module can be used in any type of signal processing application such as radar, sonar and image processing for generation of any type of signals with different frequencies. It can also be interfaced to computer, which enables the user to view or access the waveforms generated by FPGA.

REFERENCES

[1] AnudeepaS.Kholapure, Dr.ArvindAgarwal, "Design of timing signal generator for RADAR using FPGA", Second International conference on Emerging Trends in Engineering and Technology, ICETET-09, IEEE International, pp.406-409 Sept. 2009.
[2] The Design Warrior's Guide to FPGAs--Clive "Max" Maxfield.
[3] FPGA Prototyping by VHDL Examples Xilinx SpartanTM-3V ersion----Pong P. Chu.
[4] A VHDL Primer ----JayaramBhasker.
[5] Circuit Design with VHDL--- VolneiA.Pedroni.
[6] Texas Instruments DAC3283, DAC3283 Datasheets www.ti.com