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Design of Low Power Explicit Pulse Triggered Flip Flop

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Abstract: D flip flop is one of the fundamental building blocks in most digital designs. Many high speed digital circuits such as memory require high speed and low power consumption. In existing method, the charge keeper is used to provide strong 0 and strong 1 since it uses pass transistor for signal feed through technique. A new D Flip Flop is proposed with signal feed through technique using transmission gate, where the circuit of the existing method is modified for low power dissipation and to reduce the number of transistor count. The proposed method is implemented using Mentor Graphics 11.6 at 130nm Technology.

Keywords: Flip flop, Signal feed through technique, Transmission gate, Low Power

I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design [1].

Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations [3]–[8]. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Despite these advantages, pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. In [9], a statistical design framework is developed to take these factors into account. To obtain balanced performance among power, delay, and area, design space exploration is also a widely used technique [10]–[13].

II. PULSE TRIGGERED FLIP FLOP

Implicit pulse data close to output, it contains an inbuilt AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a pulse of width equal to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node X controls two larger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

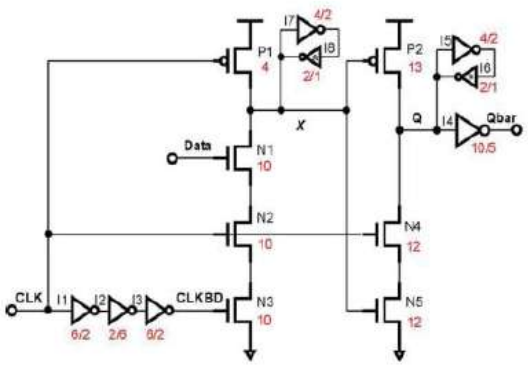

Figure.1. ip-DCO

Explicit pulsed data close to output. Fig. 2 shows a typical explicit P-FF design, named data-close to- output (ep-DCO) [3]. It contains a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node *X*. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node *X* is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation.

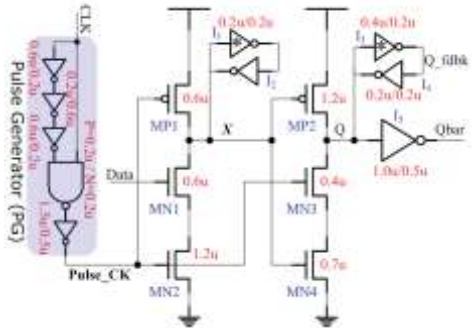

Figure .2. Ep-DCO

III. TRANSMISSION GATE

In principle, a transmission gate made up of two field effect transistors, in which - in contrast to traditional discrete field effect transistors - the substrate terminal (Bulk) is not connected internally to the source terminal. The two transistors, an n-channel MOSFET and a p-channel MOSFET are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other via a NOT gate (inverter), to form the control terminal. As with discrete transistors, the substrate terminal is connected to the source connection, so there is a transistor to the parallel diode (body diode), whereby the transistor passes backwards. However, since a transmission gate must block flow in either direction, the substrate terminals are connected to the respective supply voltage potential in order to ensure that the substrate diode is always operated in the reverse direction. The substrate terminal of the n-channel MOSFET is thus connected to the positive supply voltage potential and the substrate terminal of the p-channel MOSFET connected to the negative supply voltage potential.

IV. EXISTING P-FF DESIGN

The existing design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a

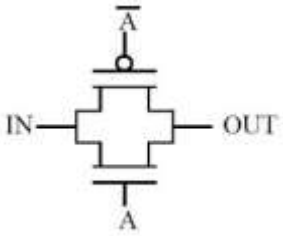

Figure .3. Transmission gate

Conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node *X* can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node *X*. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed.

Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feed through.

This scheme actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays. In comparison with other P-FF designs such as ep-DCO, CDFF, and SCDFF, the proposed design shows the most balanced delay behaviors. The principles of FF operations of the existing design are explained as follows. When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current

passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down path of node *X* is off. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs, node *X* is discharged to turn on transistor MP2, which then pulls node Q high. Referring to Fig. 4, this corresponds to the worst case timing of the FF operations as the discharging path conducts only for pulse duration. However, with the signal feed through scheme, a boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened.

Although this seems to burden the input source with direct charging/discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case because MNx conducts only for a very short period. Referring to Fig4, when a "1" to "0" data transition occurs, transistor MNx is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route.

Unlike the case of "0" to "1" data transition, the input source bears the sole discharging responsibility. Since MNx is turned on for only a short time slot, the loading effect to the input source is not significant.

In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

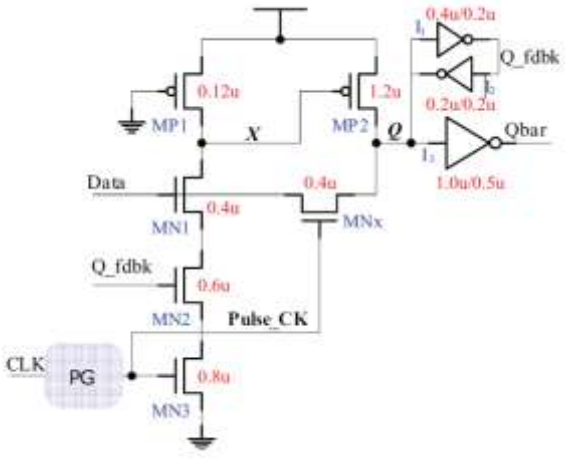

Figure .4. Schematic of the existing P-FF design.

V. PROPOSED P-FF DESIGN

The proposed P-FF design adopts signal feed through technique using TG (Transmission gate). In the existing design the signal feed through technique is employed using NMOS pass transistor, since it provides strong '1' and weak '0'.In order to provide strong '0' as well as strong '1' output a charge keeper is introduced at the output. The inverter based charge keeper is used; also the delay for the circuit is carried out through the charge keeper itself.

In the proposed method, in order to reduce the power consumption the charge keeper is removed by replacing the NMOS pass transistor by means of TG, The TG will provide both strong '0' as well as strong '1'. In order to provide delay, an inverter is placed at the output to provide feedback to the circuit. The TG is controlled through the pulse clock is included so that input data can drive node Q of the latch directly (signal feed through technique).

An inverter is placed at the output to provide the feedback, since it is a D-FF, delay is required, the delay is introduced through the feedback employed through inverter connected at the output.

Figure .5 shows the proposed P-FF design, the principle of the proposed design are expressed as follows. When a clock pulse arrived is low i.e., logic '0', the TG doesn't transfer the input data to the output, the output will be the previous data, when the clock pulse arrived is high i.e., logic '1', and the input data D is logic '0', the TG will delivers the input data to the output, since TG composed of both NMOS and PMOS, the PMOS will tack care of delivering the strong logic '0' to the output, the inverted output will given as the feedback to the circuit in order to provide the delay.

When the clock pulse arrived is high and the input data D is logic '1', the NMOS in TG will tack care of delivering the strong logic '1' to the output . When the input data, clock and the previous data's are high, the data loaded at the FF get discharged through that discharging path.

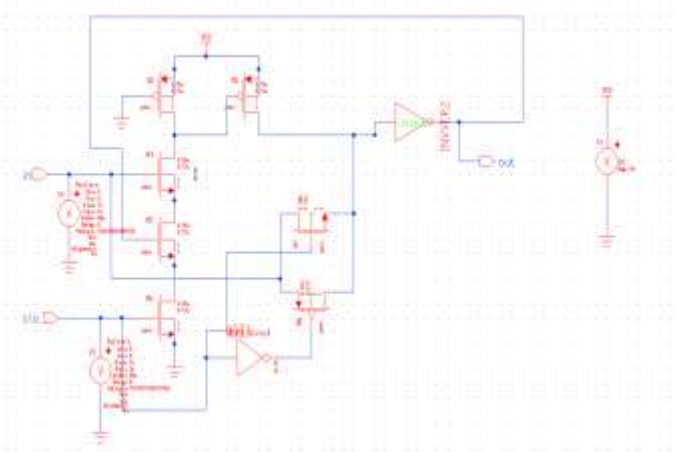

Figure .5. Schematic of the proposed P-FF design

VI. SIMULATION AND RESULT

Simulation results for proposed D-FF are shown in Figure 6 and 7. Waveform for modified explicit D-FF is shown below diagram. Input voltage for the circuit is 5V.

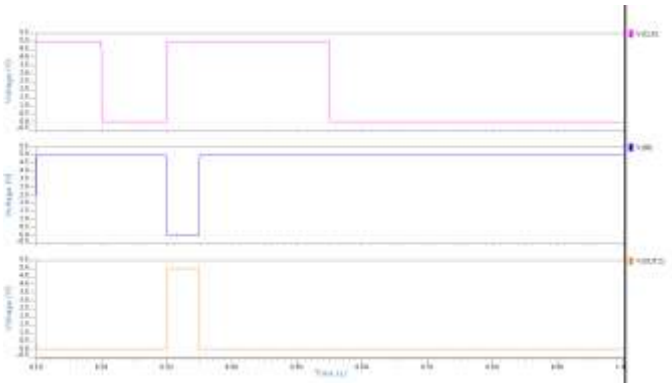

Figure .6. Output waveform of the proposed P-FF design

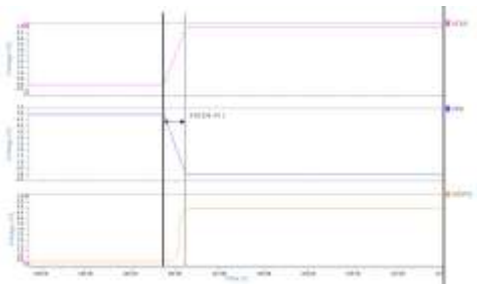

Figure.7. Delay waveform for proposed D-FF

The figure 6 shows that the waveform of input D is applied for producing the output QB with respect to the clock pulse CLK. It shows that the output voltage level is same as that of the existing method i.e.5V. The figure 7 shows that the waveform of time taken to obtain the full output

Simulation can be performed by using the Mentor Graphics. Mentor Graphics is one of the Electron Device Automation tool. In this tool Eldo, Calibre are mainly used for the simulation, LVS and DVS check. This Software is run at the LINUX operating system.

Table. I. Power and Delay for Existing and Proposed Explicit D-FF

Explicit P-FF	Transistor count	Power
Existing P-FF	12	354 nw
Proposed P-FF	11	228 nw

Table I shows the comparison of existing P-FF and proposed P-FF. Comparing with existing and proposed method power is decreased in proposed method and also the transistor count is decreased.

VII. CONCLUSION

Existing P-FF has the power dissipation of 354 nW. The same circuit is designed by using modified signal through method using TG means that the power is decreased from 354nw to 228nw .Likewise the transistor count is also reduced from 12 counts to 11 counts.

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