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Cascaded Integrator Comb Filter Design for Digital Down Converter on FPGA

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Abstract: A digitized real signal centered at intermediate frequency is converted by digital down converter to a signal centered at zero frequency. The multiplications of quadrature mixing are done at much lower rate of sampling instead of high sample rates. When there is a rate conversion of signal to a new clock frequency then there is a need of high clock rate filter architectures. At such high frequency, FIR filter variants fail to work. Cascaded Integrator Comb filters are the best choice at these high sampling rates as they support for large decimation reducing the complexity & consumption of power. CIC architecture is realized using VHDL and is simulated on Xilinx FPGA.

Keywords: CIC, digital filter, high sample rate, Integrator, Differentiator, Decimator.

I. INTRODUCTION

Varying sample rate frequency according to signal of interest is a most common procedure in signal processing. Multirate system dealt with different sampling rates. Alternative classes of FIR filter suitable for large sample rate changes are Cascaded Integrator Comb (CIC) filters. CIC filters are efficiently implemented in digital circuits. CIC filter is formed by cascading digital accumulator i.e., integrator followed by a cascade of digital differentiators (combs) in equal number. Decimator is placed in between integrator and combs to lower the frequency of comb signal with respect to system sampling frequency.

In the last decades, CIC filters have been successfully used for sample rate conversion in modern communications systems. Some modified filter structures for sigma-delta analog-to-digital applications. The novel filter classes suggested here can be used in these applications. An important measure of the performance superiority of the proposed CIC FIR filter functions is to compare them to the characteristics of the classical CIC filters. The classical CIC filters and the designed novel CIC FIR filter functions have the same number of cascaded sections with the difference that the CIC filters have an identical structure in all cascades, and the designed novel functions have a cascade-connected CIC filter sections of different lengths. Also, they have the same level of constant group delay, as well as number of delay elements, but the novel designed CIC FIR filter functions give higher insertion losses in stopband region of interest, as well as they have higher selectivity.

II. LITERATURE SURVEY

Dolecek and Mitra have proposed an efficient sharpened CIC filter of decimation for an even factor of decimation. The structure comprises of two parts: A combination of moving average filters of first order and a sharpening filter. The sharpening part is positioned to work at half of the high rate of input sampling. The poly-phase sub filters of the initial fragment can work at the 50% of the high input sampling rate, using poly-phase decomposition.

Stephen and Stewart have discussed the approaches for sharpening the frequency responses of the CIC filters. Its partially non-recursive implementation with power of 2 decimation rates 20 provides replacement to the sharpened CIC filter techniques, if considering the operating speed and compensation for the passband characteristics of a conventional comb structure is a dispute.

Uusikartano and Takala have presented a power-efficient CIC decimator structure for fs/4 down converting digital receivers. In this proposed structure power conservation is achieved by running all the integrators at half of the sampling frequency, despite the decimation ratio and the disadvantage of this structure is the increased layout area. This decimator structure is suited for any decimation ratio, even a prime or fractional number.

Rajic and Babic have proposed an efficient decimation filter structure consisting of a CIC filter with second order sharpening. This proposed structure is significantly more power efficient and appropriate to sharpening ACF due to no variation of factorization abutting ACF of linearly mixed form. In this structure, every cascaded stage is designed in non-recursive method with sharpened comb filters.

Gerosa and Neviani have been proposed a digital sinc filter formed by the convolution between the samples of input signal

and the coefficients of filter as an alternative approach to the standard CIC. This provides the eloquent decrease in hardware intricacy compared to conventional CIC.

A novel architecture for a sharpened CIC filter structure was presented by Dolecek and Mitra. This structure comprises two parts: a combination of comb filters with the down-sampling factor M1 21 and a sharpened comb filter with a factor M2 and hence M=M1M2. It permits the sharpening part to operate at a smaller rate which is M1 times lower than the high input rate and to work on a comb filter with a length M2. The first part can be realized in non-recursive or recursive form. The stop-band attenuation of this architecture not depends on M1 for a given M and this structure provides lower passband characteristics with a good stop-band attenuation compared to the practical CIC filter.

A programmable CIC based decimation filter is designed for sigma-delta ADC and manufactured in 1.5um n-well CMOS process was described by Srivastava and Anantha. The ADC scheme is demonstrated for the over sampling ratios 16 and 64 with a respective output resolution of 7 and 10 bits respectively. The programmability characteristics of the sigma-delta ADC can be extended for higher resolution further by functioning the ADC at corresponding higher decimation ratios.

Dolecek and Carmona have presented a novel improved multistage CIC-Cosine decimation filter structure. This structure is substituted by a multiple stage configuration, in which every stage comprises a cascade of CIC filter with different amount of stages. The presented filter structure is a cascade of modified CIC filter as well as cosine pre-filters. With the help of cosine pre-filters the magnitude response of this filter can be enhanced.

Dolecek and Mitra have proposed a novel sharpened comb decimation filter structure comprising of a sharpened and cascade of 22 comb-filter based decimator. Applying poly-phase decomposition to the initial stage, the sub filters can also be functioned at M1 time's lower rate. Stop-band attenuation of this arrangement not relies upon M1 for a given value of M but pass band characteristics are improved with the increase of M1.

Luis Teepanecatl-Xihuitl et al. have presented a well organized architecture for CIC based decimation filter which reduces the power considerably, by having the integrator with a poly-phase structure in which every poly-phase part works at a lowered frequency which is a complex section in multi-standard digital receivers. The voltage given to the poly-phase structure is sized to decrease the consumption of power without losing the performance of the whole structure. Various communication methods like GSM, IS-95, UMTS Mobitex and Ardis are considered in the filter design.

A novel two-stage decimation filter was presented by Dolecek. First section is the cascade of K1 in this structure, M1-length comb filters and the respective cosine filters. The next part is the cascade of K2, length comb filters and the corresponding cosine filters is M2. Selecting M1 > M 2, less power utilization is achieved compared to the case where M 2 > M 1, because in the first stage the filtering is shifted to the rate in which input rate is greater than M1. Hence the sharpening is applied only at the next stage, selecting M 2 > M 1 will yield an improved magnitude response that in the reverse case. Hence the 23 selection of decimation factors M1 and M2 relies on the compensation between the desired stop-band attenuation and the power utilization.

The design of decimation filters with low power and high precision through an efficient algorithm for sigma-delta ADC is presented by Mortazavi Zanjani et al. This algorithm is applied to the decimation filters with oversampling ratios of 32 to 256. The use of multi-stage structure with half-band filters and CIC with enhanced down-sampling approach has decreased the required amount of arithmetic calculations considerably.

Zhang and Ofner have proposed a CIC based decimation filter structure for sigma-delta ADC with low-power for GSM application with order 4 and its factor mth power of 2 and mth power of 3 poly-phase structures. The power utilization for non-recursive decimation filters with order 4 reduced about 70% contrasted to recursive structure. The design space for recursive-less decimation filters go beyond that of recursive decimation factors which have the value more than 8.

Dolecek and Mitra have intended a novel decimation filter structure, which offers better stop band attenuation around the first zero using stepped triangular impulses and cosine filters.

This proposed scheme consist two stages: The first stage comprises of polyphase decomposition and the second stage comprises the cascade of cosine filters and the CIC filter with length M2. A novel decimation filter structure is presented with a conversion factor by

Dolecek et al.in which the interpolation and 24 decimation factors are reciprocally prime numbers. This structure comprises of stepped triangular CIC and the expanded cosine filters. The expansion factor is characteristically selected to reduce the stopband characteristics of the filter. Finally it has 3 sections of integrators and/or combs and provides better performance when M1 < M 2. This exhibits better magnitude response than the modified CIC filter for software radio applications. Wang and Li proposed a decimation filter structure for reconfigurable integer factor used in SDR receiver. The fundamental concept behind this structure is that categorizing low-complexity and large-decimation-factor in initial stages and high-attenuation and low decimation-factor

components at the final stages. In this proposed structure, the CIC filters are used in initial stage as anti-aliasing filter with greater decimation factor, based on the over sampling rates in various stages as final stages, Nyquist and equiripple half band filters are used.

III. CIC FILTER

Fig.1 illustrates the digital down converter architecture with CIC filter.

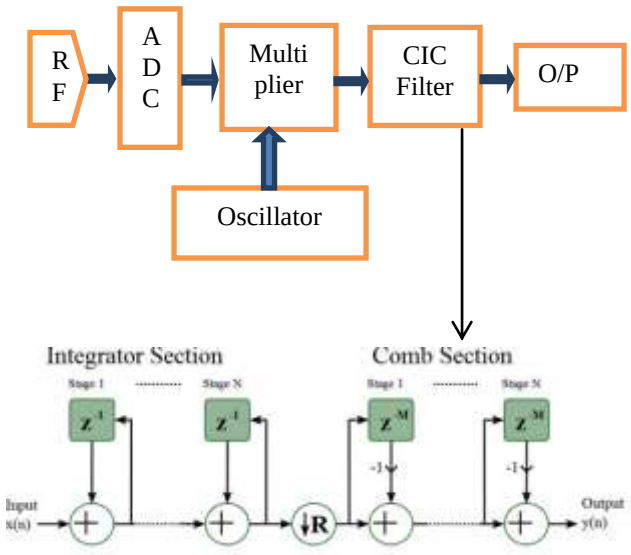

Fig.1. DDC architecture

CIC filter consists of same number of integrator and comb sections. An integrator is IIR filter with single pole and unity feedback coefficient which is also called accumulator.

The output response of an integrator is basically an LPF with infinite gain at DC. The output can increase with a finite input which means a single integrator is unstable. A comb filter operates at high sampling rate and realize by adding a delayed version of signal to itself causing interference.

In CIC filter, by cascading N integrator and N comb sections the efficiency grows by slowing down half of the filter, cut down the delay elements essential in the comb section and comb and integrator section are independent of rate changer.

IV. SIMULATION RESULTS

The proposed CIC filter is modeled in VHDL (Very High speed Integrated Circuit Hardware Description Language) language and simulated in Xilinx ISE (Integrated Software Environment) tool. The CIC filter is implemented on the Xilinx spatan3 XC3S400PQ208 device. The below figure 2 shows the RTL (Register Transfer Logic) schematic of the CIC filter. After synthesizing Verilog HDL of CIC filter the total design is represented in Gates and Multiplexers The internal architecture of RTL is shown in below figure 3.

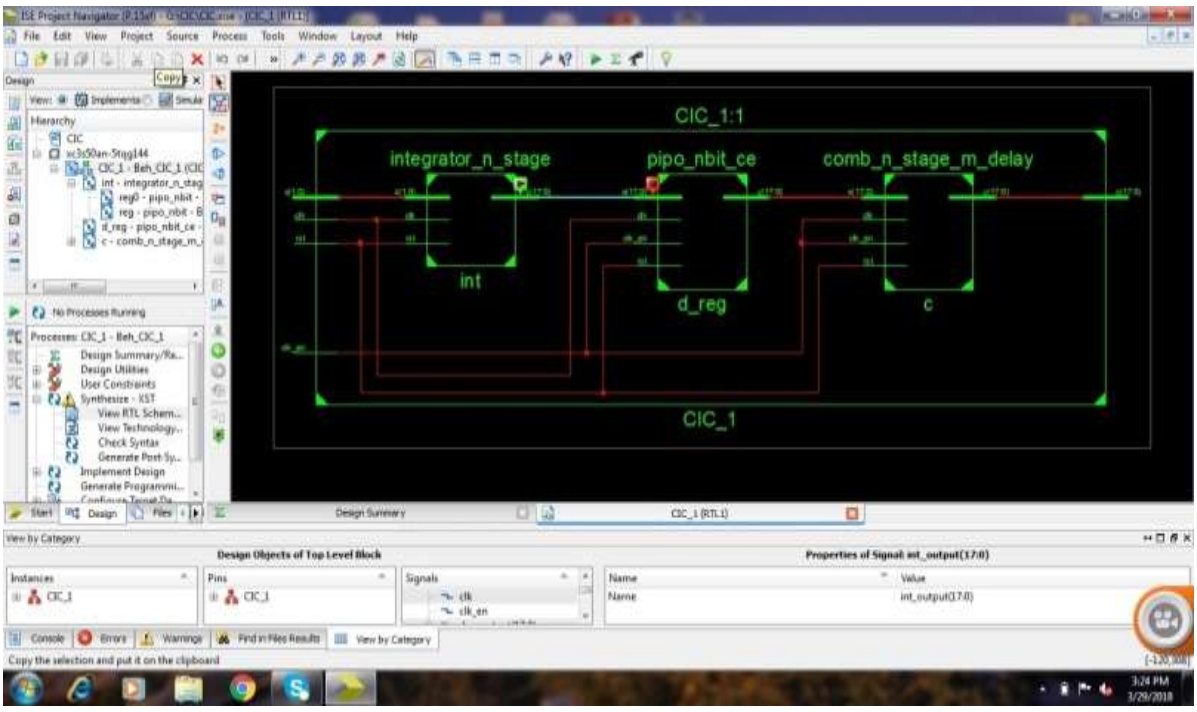

Fig.2. RTL schematic

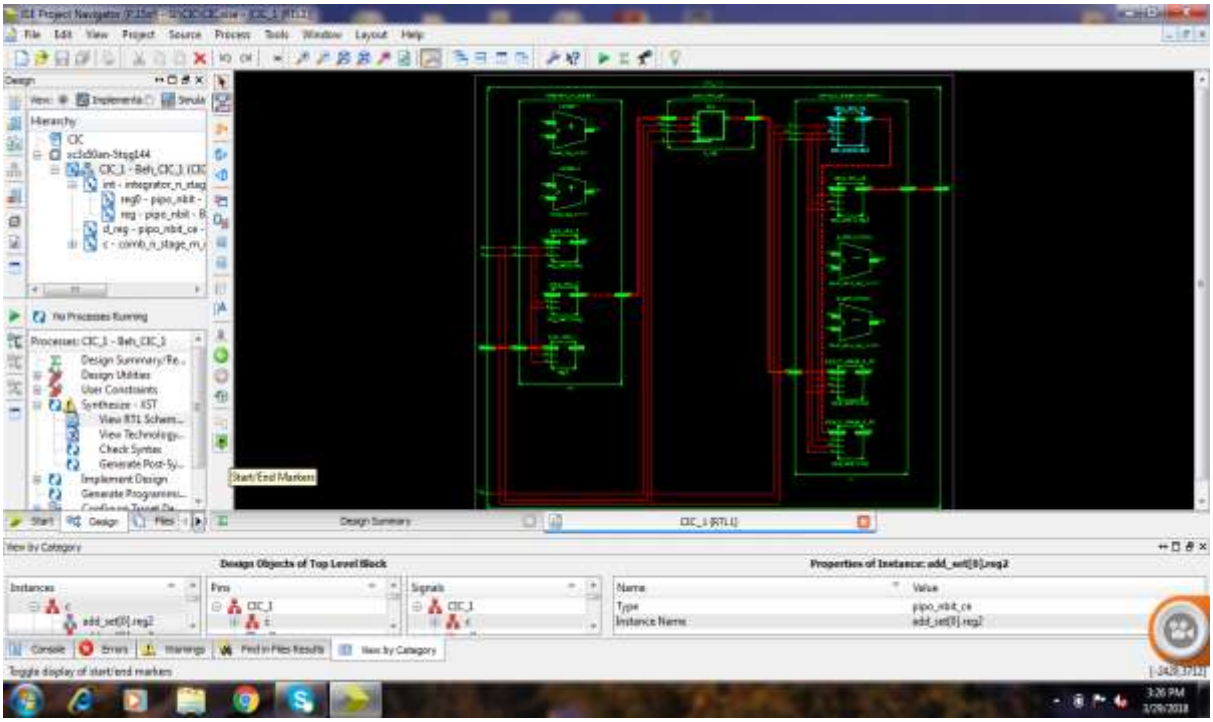

Fig.3. Internal architecture of RTL

The technology schematic of CIC filter will be mapped to LUTs (Look Up Tables) present in Xilinx FPGA board. The technology schematic of CIC filter is shown in below figure 4.

The CIC filter is simulated in Xilinx ISE simulator where the Simulation output of the CIC filter is shown in the below figure5.

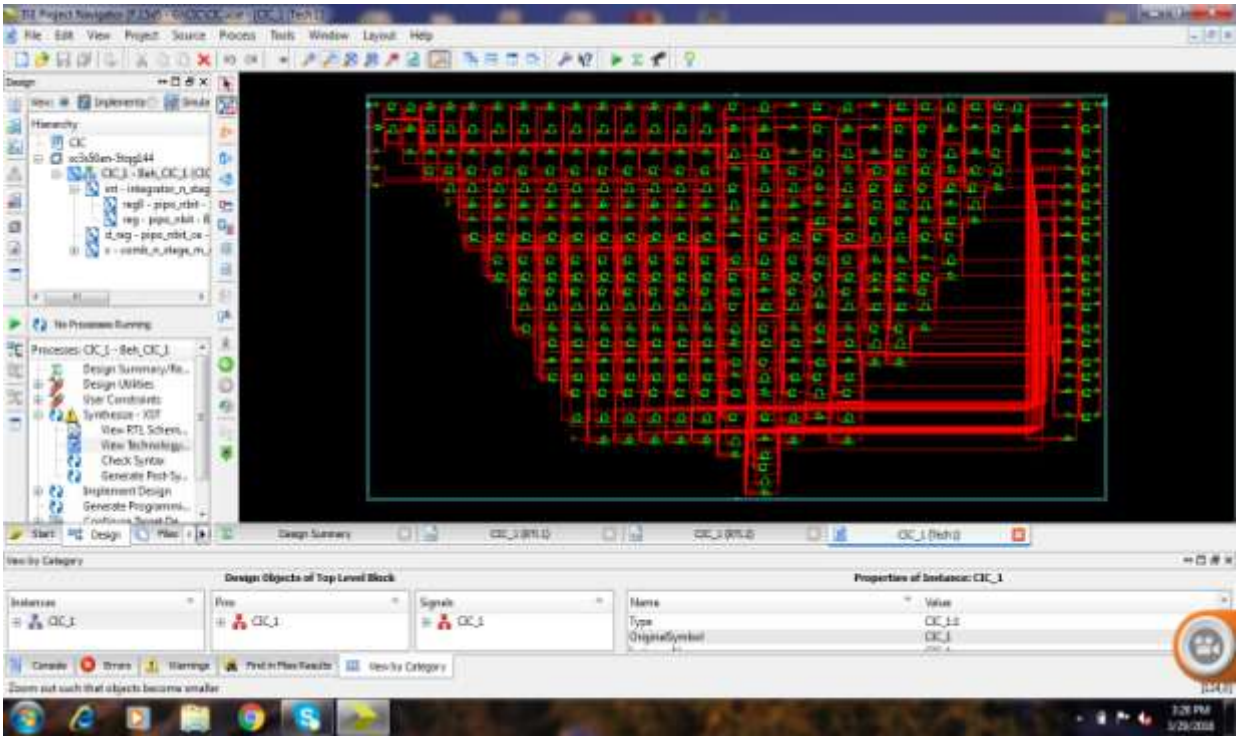

Fig.4. Tech schematic internal architecture

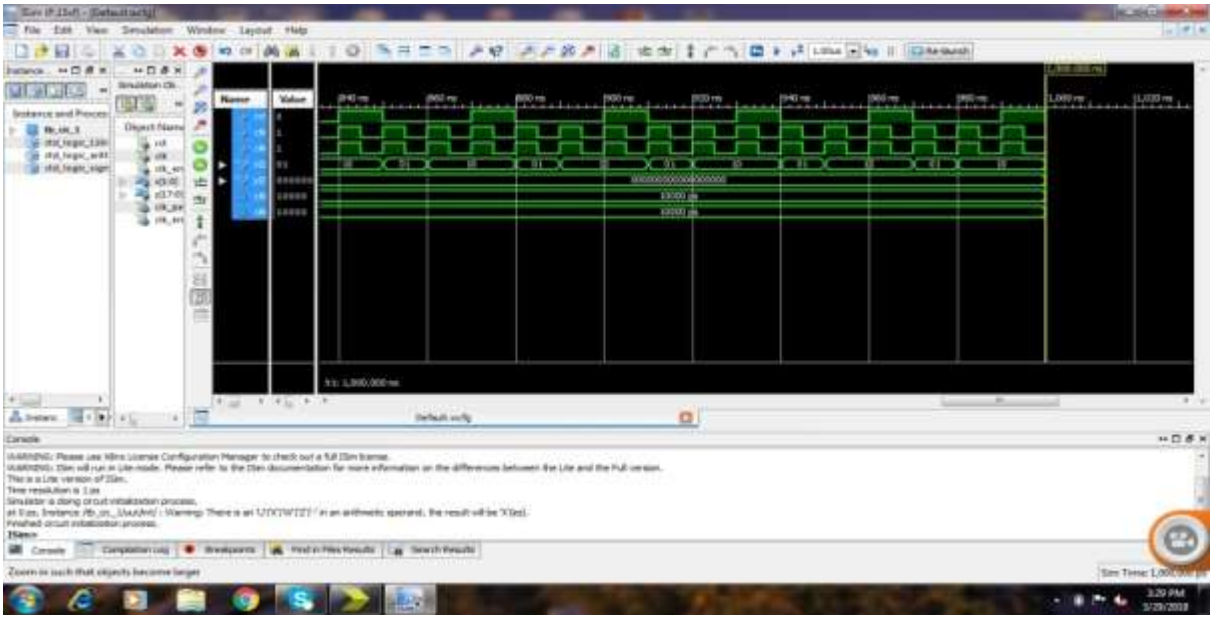

Fig.5. CIC simulation output

V. CONCLUSION

The narrow band construction and extraction plays an important role in data processing this can be achieved by Interpolation and decimation process. This is accomplished by Cascaded integrator combo filters called CIC filter. CIC filter was modeled using VHDL language and simulated in Xilinx ISE tool. For new CIC filter the simulation results are taken for decimation factor or M=8 and 16. The realization of CIC filter will reduce the device utilization area and power consumption.

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