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Design and Implementation of Flash ADC Using Precise Comparator

R Sindhu
Department of ECE VEMUIT
VEMU Institute of Technology
Chittoor, India
E-mail: sindhuadithya2017@gmail.com

Abstract: A low-power comparator is presented. PMOS transistors are used at the input of the preamplifier of the comparator as well as the latch stage. Both stages are controlled by a special local clock generator. At the evaluation phase, the latch is activated with a delay to achieve enough pre amplification gain and avoid excess power consumption. Meanwhile, small cross coupled transistors increase the preamplifier gain and decrease the input common mode of the latch to strongly turn on the PMOS transistors (at the latch input) and reduce the delay. Unlike the conventional comparator, the proposed structure let us set the optimum delay for pre amplification and avoid excess power consumption. The speed and the power benefits of the comparator were improved. A Flash ADC is designed using this proposed comparator. Flash ADC is the fastest among the entire analog to digital converters. The designed flash ADC can achieve high speed and low power consumption.

Keywords: ADC- Analog to Digital Converter, PMOS- P type Metal Oxide Semiconductor, clk-clock

I. INTRODUCTION

Nowadays, ADCs are being used in a huge range of applications such as communication systems, biomedical implants, and digitally assisted analog circuits. Needless to say, comparators are one of the most effective blocks of commonly used ADCs such as Flash, SAR, and Pipeline ADCs. Recently the need for low-power high- speed ADCs has increased dramatically and these are integral parts of a variety of applications such as handheld devices. Comparators are the key building blocks of different types of ADCs, such as SAR, pipeline, and flash ADCs. Several years ago, CMOS amplifiers were used as static comparators, although they suffer from very high power consumption (since they are always on) and inherent limited speed (since they have no positive feedback).

II. LITERATURE SURVEY

Shilpi Singh-International Journal of Microelectronics Engineering(2015),ANOVEL CMOS DYNAMIC LATCH COMPARATOR FOR LOW POWER AND HIGH SPEED

The power problem is one of the most serious limitations in high performance VLSI‟s and battery backed-up systems. High speed and low power comparators are the essential building blocks of many analog circuits such as high speed analog-to-digital converters (ADCs), memory sense amplifiers and data receivers. In analog to-digital converters, the comparator plays a vital role on the overall performance of the converter. A fast and accurate comparator is a crucial element in any high resolution and high speed data converters. There are two main types of comparator based on their structure and operation: amplifier chain type and latch type. Amplifier chain-type comparators use a set of cascade amplifiers to generate the output in response to small difference

Between input signal and reference signal. On the other hand, latch type comparators provide higher speed and lower power consumption.

III. EXISTING METHOD

The existing comparator uses a PMOS latch which is activated with a predetermined delay during the evaluation phase. This delay is supposed to be the optimum delay. At the reset phase, the clk, clkb1, and clkb2 hold logic 1 to discharge the output voltages of both preamplifier and latch to GND. At the evaluation phase, first the clk and clkb1 are toggled to logic 0‖ to start pre amplification (charging the parasitic capacitors of O1+ and O1− nodes differentially). During this phase, the cross-coupled circuit increases the differential voltage (Vidl = [VO1+−VO1−]) slowly (since M4,5 are mostly in sub threshold region) and reduces the common mode voltage (Vcml = 0.5 ×[VO1+ + VO1−]) to provide a strong drive for the input PMOS latch stage. Increasing Vidl (means larger preamplifier gain) further eliminates the effect of the latch on the input referred offset voltage. Also, larger Vidl results in a smaller latch delay. Decreasing Vcml enhances the speed of the comparator, since PMOS transistors are used at the input of the latch .

Finally, clkb2is toggled to logic 0 to activate the latch. Simultaneously, clkb1 is changed to logic 1 to turn off the current source of the preamplifier in order to avoid excess power consumption. Amplification of Vid is kept going during this phase because the cross coupled circuit is still working independently of the current source (M8). Meanwhile, Vcml is kept reducing by M3−5. The control signals are implemented

using a local clock generator as which consumes a small amount of power. The black inverter is designed carefully to adjust the delay. Instructively, the proposed comparator is robust against overlapped control signals, since overlapped signals only slightly affect the power consumption and have no effect on the precision. In the proposed circuit, the delay of the evaluation-phase is long enough to achieve the minimum required preamplification gain for a given speed and latch offset elimination than x to cross coupled circuit (M3−5), during the first step of the evaluation phase, the differential voltage at O1+ and O1-nodes increases; however, the common- mode voltage of those nodes is kept low.

Therefore, for a suficient evaluation phase delay, tamp, Vcml (= 0.5× [VO1+ + VO1−]) is pulled down to activate the PMOS latch strongly. Also, the larger Vidl boosts the latching process (speed). Consequently, the delay of the comparator will be small and almost flat over a wide range of the input Vcm. Transition of clkb1 to logic 1 limits the power consumption of the preamplifier which is the main part of the total power consumption.

In the meanwhile, the cross-coupled circuit continues preamplification at no cost of power consumption. As another Benefit, the delay time from beginning of the evaluation phase to beginning of the latching process is simply controllable and can be tuned at its optimum value. However, in the conventional comparator, delay is inevitably fixed to the required time to charge the output parasitic capacitors of the preamplifier to the level of an NMOS voltage threshold.

The proposed structure can also be implemented using NMOS transistors, i.e., latch and preamplifier with input NMOS transistors. This will result in a higher speed because of the inherent superiority of NMOS transistors over PMOS ones. The size is chosen large enough to keep the output common-mode voltage of the preamplifier small enough and increase the preamplifier differential gain. In this paragraph, the core concept of the proposed comparator is briefly described.

In the conventional comparator, if the preamplifier and the latch work in different time slots, the power consumption is improved. To do this efficiently, one way is to change the structure of the conventional comparator.

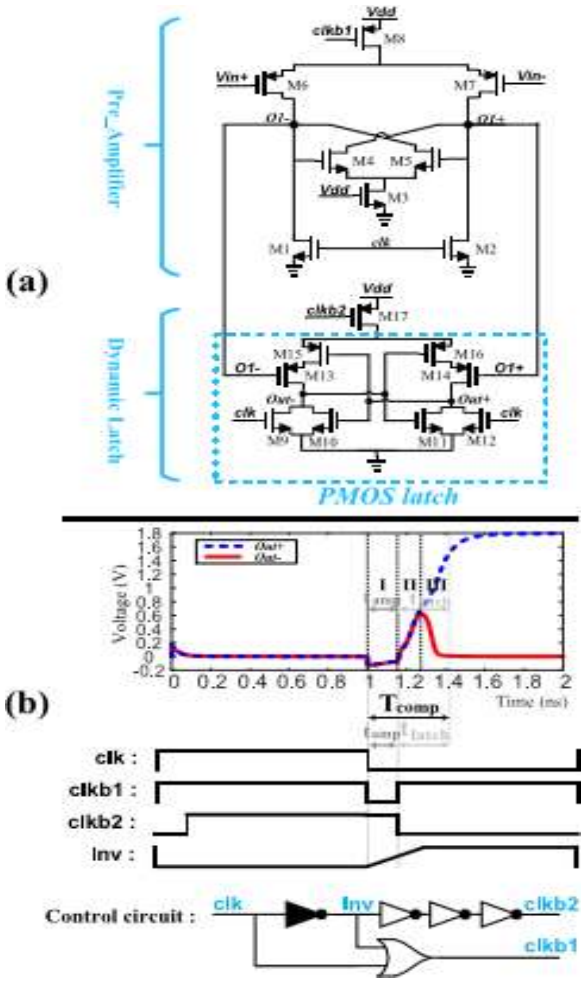


FIG. (a) Two-stage dynamic comparator. (b) Its typical output waveform and clock signal

IV. PROPOSED FLASH ADC

A high-speed flash ADC needs (2^N – 1) comparators for an N-bits conversion. Folding technique reduces the number of comparator by dividing the ADC to coarse and fine parts. The folding operation is normally performed using an amplifier which consumes lots of static power especially for high speed applications and large folding factor. Interpolation technique reduces the number of pre-amplifiers and thus reduces input capacitance. However, number of latches is same as flash topology. Changing reference voltages of comparators depending on input voltage can be used in order to reduce number of comparators. In this structure, N-bit conversion needs only N comparators. As illustrated for a four bit ADC, reference

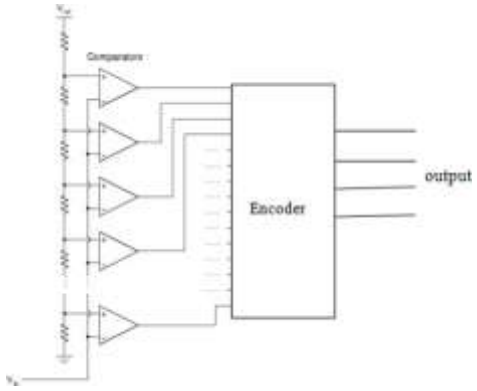
voltage of each comparator changes regarding to the higher priority comparator.

In fact, this technique introduces an appropriate trade-off between speed and power consumption. In comparison with typical flash topology this structure consumes less power. However, it is slower because of sequential behavior of comparators outputs. In other words, operation of this structure is same as a SAR ADC. Nevertheless, while a SAR ADCS performs a conversion using a comparator along with a Digital to Analog Converter (DAC), this structure uses N comparators for N bits conversion with the advantage of higher speed. Since the digital part of an SAR ADC consumes a significant power in high-speed applications, power consumption of this structure As a result, this topology needs the static comparators to work properly. However, static comparators consume lots of power which is unlike the idea of this topology; reduction of power would be comparable with SAR ADCs as this structure does not need the digital part. In order to perform a full conversion, each comparator should update its output as soon as its inputs change. Consumption of conventional flash ADCs. The modified structure is proposed to reduce the power consumption topology using dynamic comparators. Dynamic comparators complete a comparison in two phases; pre-charge phase and evaluation phase. Dynamic comparators are initialized for comparison during pre-charge phase and then, comparison starts in evaluation phase. Consequently, the inputs of dynamic comparators should be ready before beginning of the evaluation phase. A clock generation chain is used to guarantee that evaluation phase of each comparator starts after preparation of comparator inputs. The comparators are in pre-charge phase when clock input is high and turn to evaluation phase when clock signal goes low. Since the pre-charge phase needs lower time in comparison with the evaluation phase, a variable pulse generator is used to reduce the pre-charge time and increase the evaluation time.

WORKING:

In flash ADC, Analog voltage is applied to non inverting terminals of all comparators using a single line. In figure 4.1, Reference voltage is applied to

FIGURE : PROPOSED FLASH ADC



Inverting terminals of comparators using divider circuit. Each comparator produces digital output in the form of 1 or 0. If unknown analog voltage is greater than reference voltage comparator produces high logic. If analog voltage is less than reference voltage then comparator produces low logic i.e. 0.Thus all parallel comparator produces digital

Representation of analog voltage in the form of zero and one. These outputs of comparator are then applied to the fast encoder. Encoder converts those zeros and once into binary number and produces digital binary output.

	Comparator using NMOS	Comparator using PMOS
Power(uw)	217.9377	202.338
Delay(ns)	9.8402	1.1684

TABLE 1. **COMPARISON TABLE OF EXISTING METHOD**

By the above comparison we came to know that the comparator which uses PMOS as latch is having less delay and less power consumption than the comparator which uses NMOS latch.

SCHEMATIC OF PROPOSED FLASH ADC

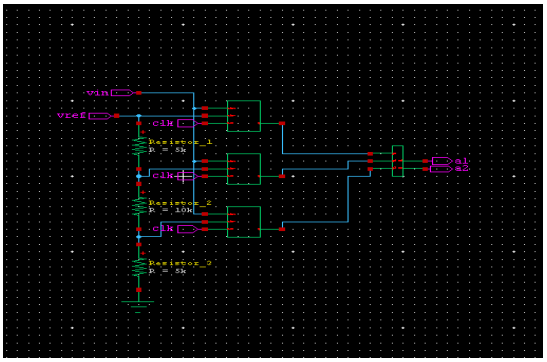


Fig: Schematic of Proposed 2 bit flash ADC

SIMULATION OUTPUT OF COMPARATOR

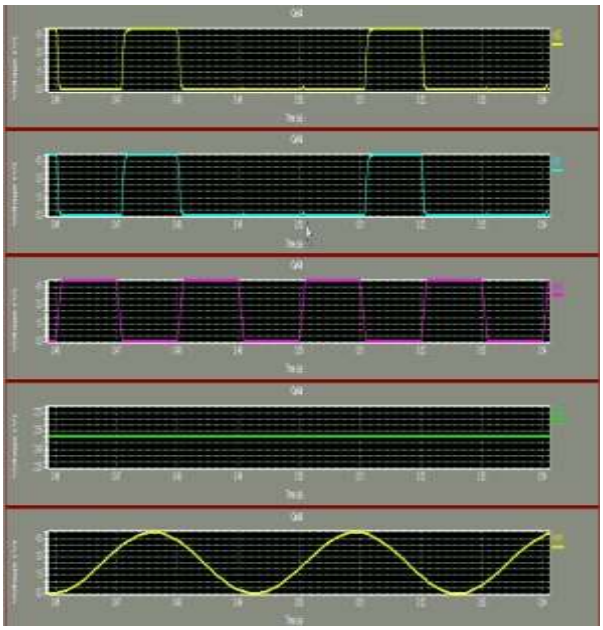


Fig: Simulation output of Comparator

SIMULATION OUTPUT OF FLASH ADC

The encoder outputs are digital signals. Here we are getting three digital signals at different levels from bottom to top: input signal, reference voltage, clock signal, comparator outputs at 5kohms, 10kohms, 20 kohms.

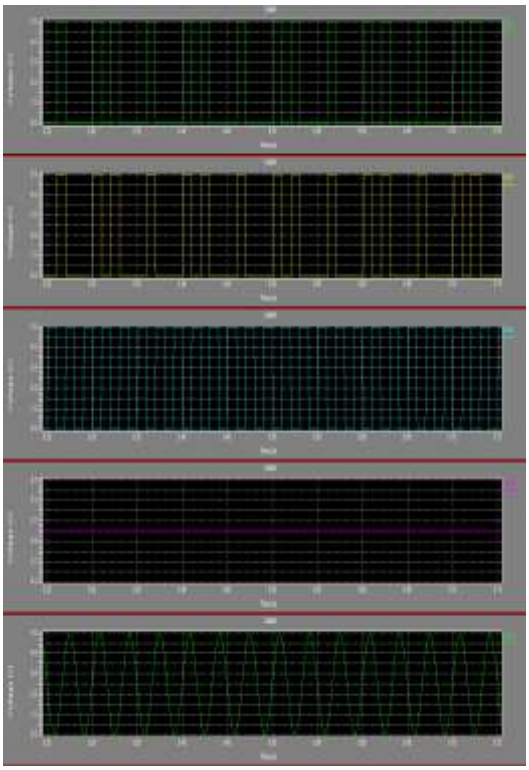


Fig: Simulation output of Flash ADC

V. CONCLUSION

In the comparator, PMOS latch and PMOS preamplifier in addition to a small cross- coupled circuit are used with a special clocking pattern to adjust the preamplifier gain. The clocking pattern provides enough preamplifier gain; since PMOS transistors are used at the input of the latch, and the cross-coupled circuit is employed to keep the common mode voltage of the preamplifier outputs at a low level. The speed of the comparator is increased and is constantly high for a wide input Vcm range. Deactivating the preamplifier after the optimum delay reduces the power consumption significantly.

VI. FUTURE SCOPE

All the parameters of reconfigurable flash ADC can be considered for lower resolution and compare its characteristics with other low resolution ADCs. Offset cancellation technique can be adopted in order to reduce the offset in the comparator which improves the efficiency of the total flash ADC. Calibration technique shows great potential in high speed and low power flash ADC design. This technique can be adopted in order to simplify the design.

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AUTHOR'S BIOGRAPHIES

Mrs. R SINDHU, M.Tech.,
ECE DEPARTMENT
Assistant Professor
Vemu Institute of Technology