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Quaternary Lookup Table (QLUT) Based Digital Applications

Ms. M. Mani kumari
(Assistant Professor)
Electronics and Communication
GVP college of Engineering for Women
Visakhapatnam, India
E-mail: mani.kumari@gvpcew.ac.in

Ms. M. Alekhya
Electronics and Communication
GVP college of Engineering for Women
Visakhapatnam, India
E-mail: maddulaalekhya16@gmail.com

Ms. P. Sahithi
Electronics and Communication
GVP college of Engineering for Women
Visakhapatnam, India
E-mail: sahithipakanati@gmail.com

Ms. K. Sireesha
Electronics and Communication
GVP college of Engineering for Women
Visakhapatnam, India
E-mail: kuppilisireesha1@gmail.com

Abstract: In today's world VLSI chips are widely used in various branches of Engineering like Voice and Data communication networks, Digital signal processing, Computers, Commercial Electronics, Automobiles, Medicine and many more. So, there have been major advances in IC technology which have both made feasible and generated great interest in electronic circuits which employ more than two discrete levels of signals such circuits called Multiple valued logic circuits, offer several potential opportunities for the improvement of present VLSI circuit designs. Multi valued logic can carry more information on a single line. The key benefits of MVL are increased data density, reduced dynamic power dissipation and chip area.

The major area of binary logic IC's are occupied by the interconnections. The more effective utilization of interconnections is possible which uses a larger set of signals over the small area in MVL devices. The higher radix in use is the ternary (radix - 3) and Quaternary (radix - 4). The Quaternary logic uses 0, 1 , 2 and 3 logic levels. In this project a new lookup table is proposed where information is represented by quaternary values known as Quaternary lookup table. By using this designed quaternary lookup table different digital applications are developed using Mentor graphics tool.

Keywords: Look Up Table (LUT), Quaternary Logic, Standard CMOS technology, Multiple-Valued Logic (MVL)

I. INTRODUCTION

The inventions of the transistor brought about a giant technology leap in microelectronics. With the advent of the transistor and, decades later, with the arrival of the integrated circuit, power dissipation became a lesser concern. Greater emphasis was placed on performance and miniaturization, yet power dissipation was not entirely ignored. To improve the performance of the circuits and to integrate more functions into each chip, feature size had to shrink more and more. Even with the scaling down of supply voltage, power dissipation has not diminished since higher levels of integration also allows for more functionality.

In recent years, there have been major advances in integrated circuit technology which have both made feasible and generated great interest in electronic circuits which employ more than two discrete levels of signal. Such circuits, called multiple-valued logic circuits, offer several potential opportunities for the improvement of present VLSI circuit designs.

II. MULTIPLE VALUED LOGIC

The logic circuitry that deals with more than two logic levels is termed as -multiple valued logic. This is also called multiple value logic system or many valued logic system Currently there are ternary logic and quaternary logic. Ternary logic system contains 3 input logic levels different from quaternary and binary. Based on the representation of logic levels, the ternary logic system is categorized into two types. They are simple ternary and balanced ternary. Simple ternary has the logic values 0, 1, and 2 whereas the balanced ternary has the logic values -1, 0, and 1.

Quaternary logic system As against binary gates have two logic levels {0,1}. quaternary gate has four logic levels{0, 1, 2, 3} in input and output. Hence the following combinations could be

{(0,0), (0,1), (0,2), (0,3), (1.0), (1,1), (1,2), (1,3), (2,0), (2,1), (2,2), (2,3), (3,0), (3,1), (3,2), (3,3)}

available at input and corresponding output according to algebras define.

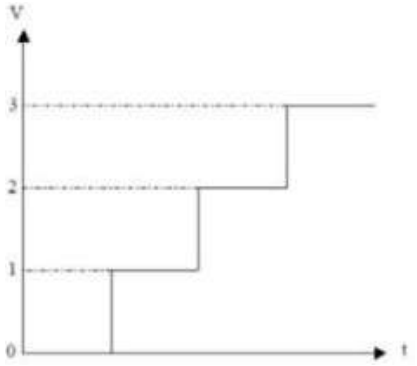


Figure Shows The Graphical Representation Of Quaternary Logic

Importance of MVL logic:

In a typical binary VLSI circuit, interconnect accounts for 70% of the chip's area while the processing transistors occupy only 10% of the chip. The remaining 20% is devoted to insulation. Thus the design of the binary logic circuits is limited by the requirement of the interconnections. A more cost effective way of providing interconnections could thus be of great benefit. One of the most promising approaches to solve these interconnection problems is the use of multi-valued logic (MVL) inside the VLSI chip. Multiple-Valued Logic system is one of the most promising approaches to realize future beyond-binary electronics and systems. One possible solution can be achieved by using a larger set of signals over a similar chip area, such as multiple-valued logic (MVL) devices. Multiple-valued logic can provide improved circuit interconnections, reduced chip area and increased bus efficiency, since more logic levels are used per line as compared to conventional binary logic.

The current trend in Integrated Circuits (IC) is to embed multiple systems into a single IC, known as System On a Chip (SoCs) leading to, among other things, an increment in the quantity, the delay time, length, and complexity of the interconnections. The multiple valued logic is a viable alternative to cope with the interconnections issues as they decrease the number of the interconnections as the inverse of the Log_2M. This reduction in the area of the IC devoted to the interconnections has motivated many MVL proposals. In the field of computing, MVL logic can lead to significant improvement because of its higher information capacity and requiring less circuit blocks per symbol compared to the binary systems.

QUATERNARY LOGIC AND LUT

A quaternary variable can assume four different logic levels. Assuming a rail-to-rail voltage range and equal noise margins for the four logic levels, three different reference voltage values are required, 1/6VDD, 3/6VDD, and 5/6VDD, to determine a quaternary value. This is shown in Fig below. Since a quaternary variable (Q) is able to carry twice information as a binary variable (B), we have the following relation: $|Q| = 2 \times |B|$.

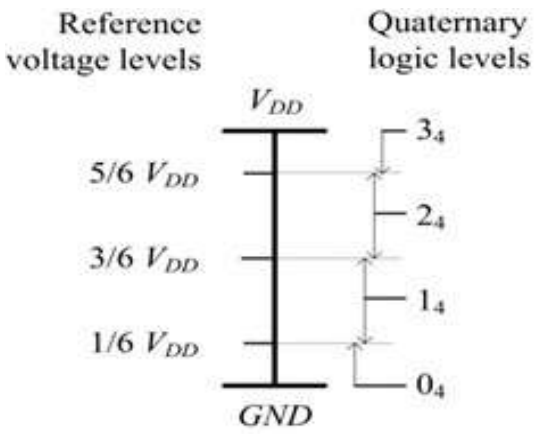
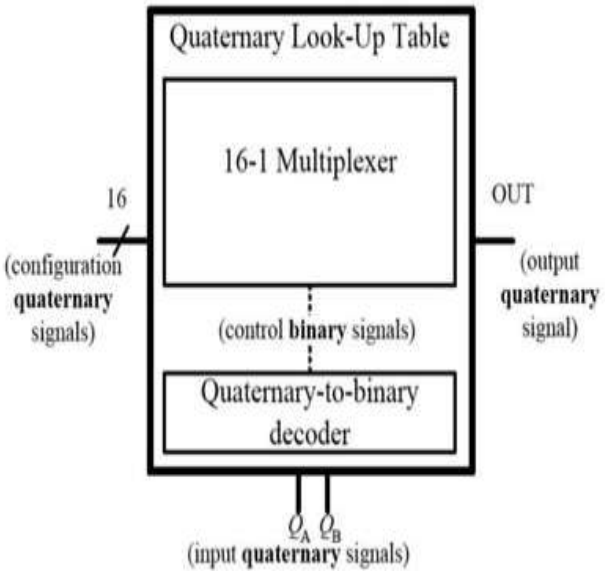


Fig: Quaternary logic and reference voltage levels



A LUT is an array indexing operator, where the output is mapped by the input, based on the configuration memory. The configuration values are initially stored in the LUT configuration memory, and according to the input, the logic

value in the addressed position is assigned to the output. By properly programming the LUT configuration memory, the LUT can implement any logic function with the given number of inputs and outputs, making it very practical to implement reconfigurable hardware, such as FPGAs. The 2-input 1-output QLUT is shown above.

III. QUATERNARY LOGIC GATES AND THEIR SIMULATIONS

In order to generate a QLUT we need a quaternary to binary decoder and a 16:1 multiplexer. For designing a quaternary to binary decoder we require basic building modules of

1.Quaternary inverter

2.Self referenced comparators

i.CP circuit

ii.CN circuit

3.Quaternary NAND

4.Quaternary NOR

Design equations to calculate aspect ratio :

Inorder to generate four different logic levels for quaternary we need to have different aspect ratios for different circuits. These aspect ratios can be obtained from the below equations.

$$k_n/k_p=(V_{dd}+V_{to,p}-V_{th})^2/(V_{th}-V_{to,n})^2$$

where V_{dd} is operating voltage,

V_{th} is threshold voltage,

$V_{to,p}$ is threshold value of p channel,

$V_{to,n}$ is threshold value of n channel,

k_n and k_p are n and p constants.

$$k_n/k_p=\mu_n C_{ox}(w/l)_n/\mu_p C_{ox}(w/l)_p$$

where μ_p is mobility of pmos,

μ_n is mobility of nmos,

C_{ox} is oxide capacitance.

For different values of $V_{to,p}$ and $V_{to,n}$ the ratios of the aspect ratios can be calculated.

1.Quaternary inverter:

The quaternary logic inverter requires 5 NMOS and 5 PMOS. The schematic is designed in MENTOR TOOL tool for 130nm technology.

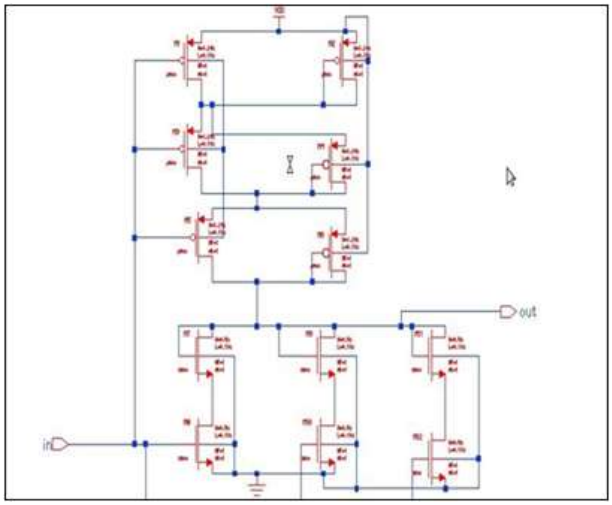


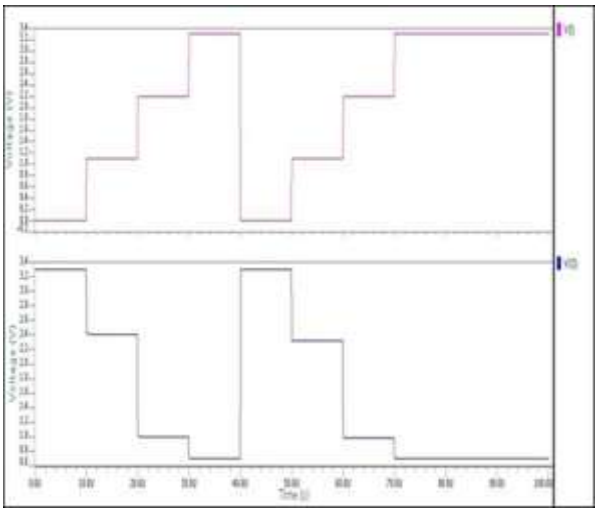
Figure: schematic of quaternary inverter

Transistor	Length	Width
PMOS	0.13u	3.24u
NMOS	0.13u	0.5u

Truth Table:

Xi(i/p)	Xo(o/p)
0	3
1	2
2	1
3	0

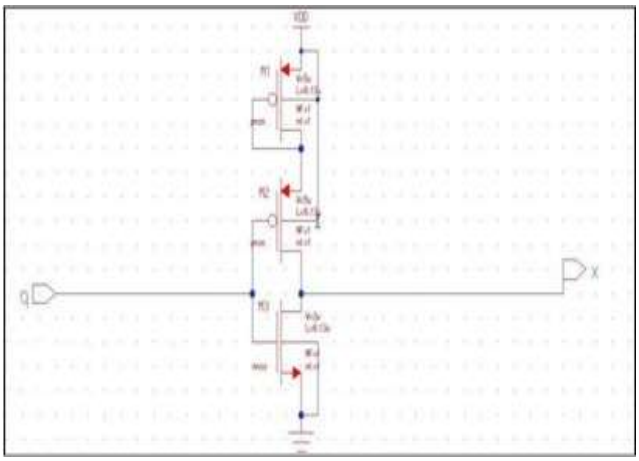
Functionality of quaternary inverter



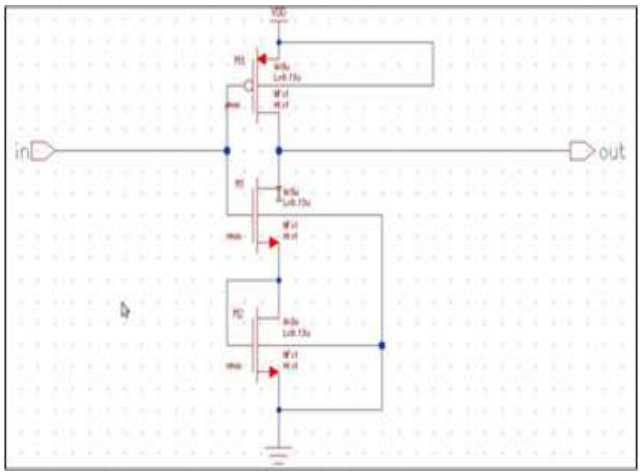
2.Self referenced comparators:

The CP and CN are self-reference analog comparators shown below. With these structures we are able to detect the four possible voltage levels.

i.CP CIRCUIT:

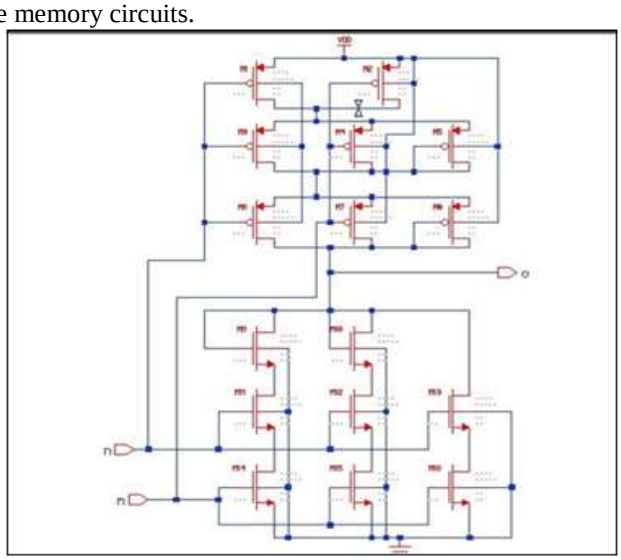


ii.CN CIRCUIT:



3.Quaternary NAND:

Quaternary NAND gate is also an elementary form of various logic circuits. Like inverters and NOR, it can be used to realize the memory circuits.



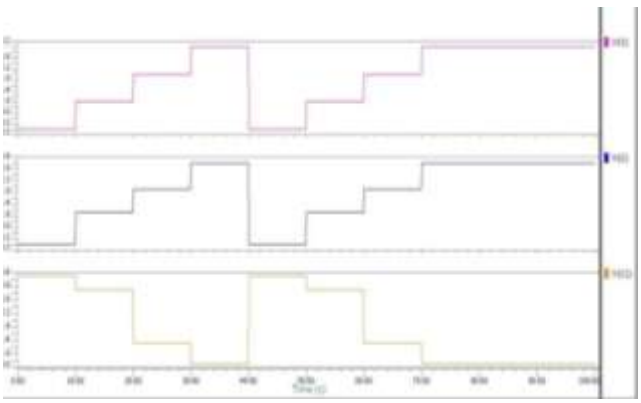
Schematic of quaternary NAND circuit

TRANSISTOR	LENGTH	WIDTH
PMOS	0.13U	0.7U
NMOS	0.13U	0.5U

TruthTable:

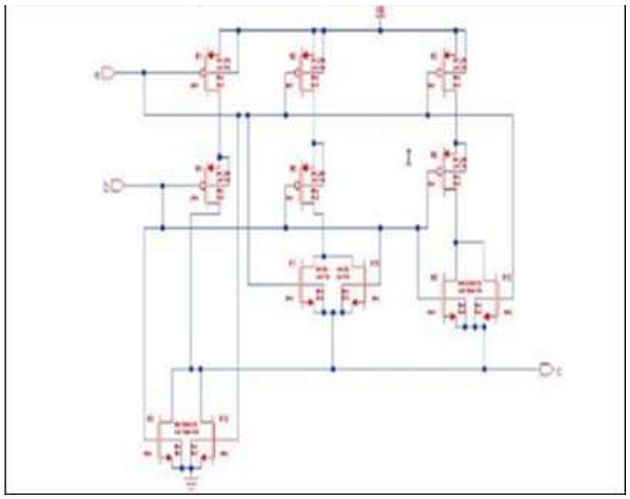
In1 / In2	0	1	2	3
0	3	3	3	3
1	3	2	2	2
2	3	2	1	1
3	3	2	1	0

Functionality of Quaternary NAND:



4. Quaternary NOR:

Quaternary NOR can be used to realize the memory circuits such as flip-flops. By using flip-flops shift registers and counters can be designed

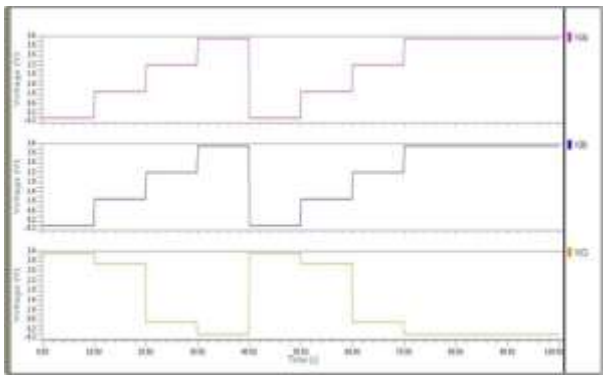


TRANSISTOR	LENGTH	WIDTH
PMOS	0.13U	3.24U
NMOS	0.13U	0.5U

Truth Table:

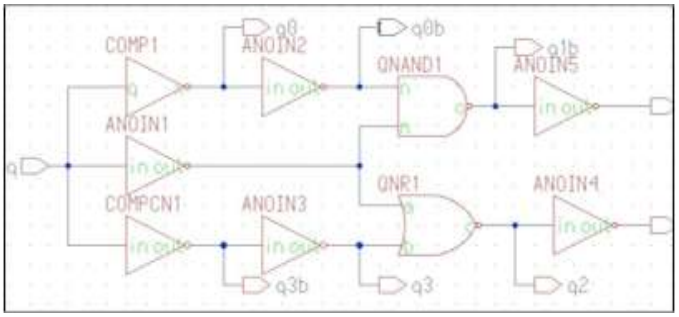
In1 / In2	0	1	2	3
0	3	2	1	0
1	2	2	1	0
2	1	1	1	0
3	0	0	0	0

Functionality of Quaternary NOR:



IV. QUATERNARY TO BINARY DECODER:

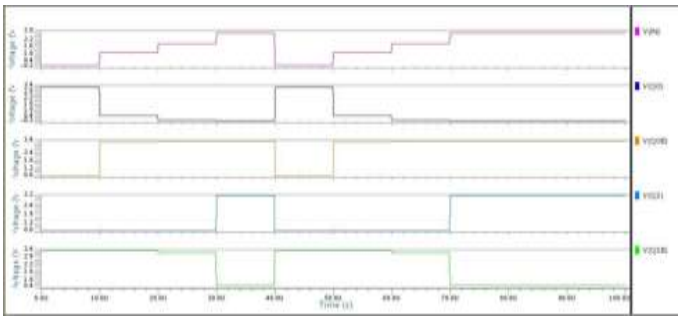
The Q-decoder outputs may be considered as flags that determine which quaternary value is applied to Q-decoder input. Once we are able to determine the quaternary value in the Q-decoder input Q, the transmission gates connected to the Q-decoder outputs may be properly controlled. In other words, with the Q-decoder structure we are able to convert a quaternary input to a 4-bit word in one-hot codification and its inverted value.

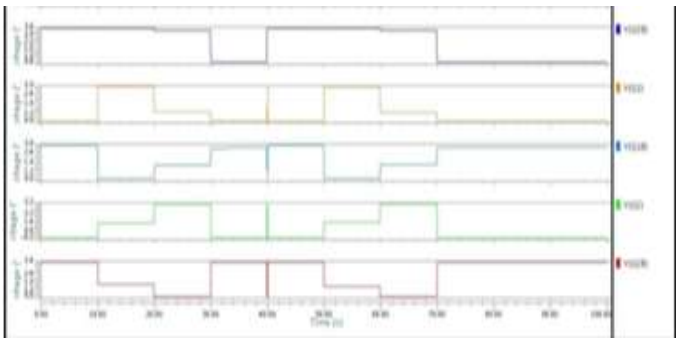


Truth Table:

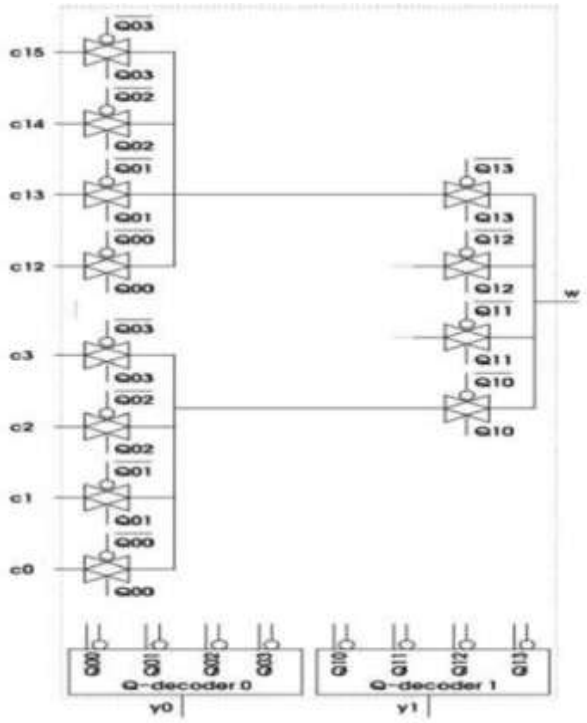
Q	Q_0	Q_1	Q_2	Q_3
0_4	1_2	0	0	0
1_4	0	1_2	0	0
2_4	0	0	1_2	0
3_4	0	0	0	1_2

Functionality of decoder:

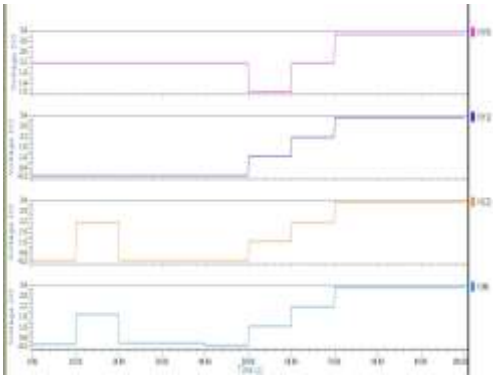


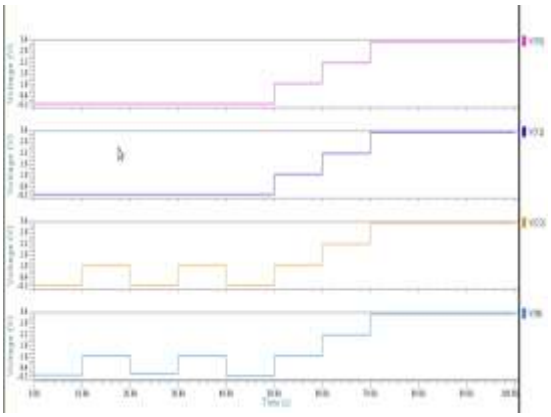


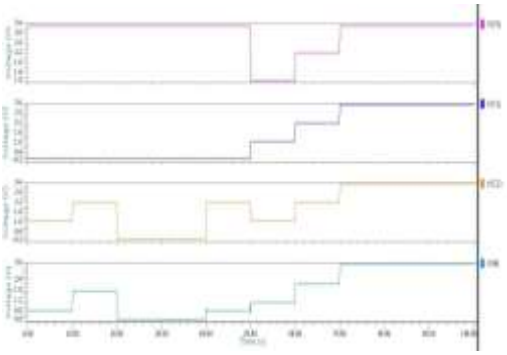
V. QUATERNARY LOOK UP TABLE



Functionality of QLUT:







VI. CONCLUSION

This work has aimed at the design and implementation of an innovative QLUT design that can be used for multiple valued combinational logic or as a building block in FPGAs. The use of multiple valued logic inside a VLSI chip leads to decrease the number of interconnections which further leads to the reduction in the chip area, delay and crosstalk noise.

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AUTHOR'S BIOGRAPHIES

Ms. M. Mani Kumari currently an Assistant Professor of Electronics and Communication Engineering at Gayatri Vidya Parishad College of Engineering for Women, Visakhapatnam, Andhra Pradesh and pursuing Ph.D (Part-time) in jntuk University. Her teaching experience is around 10+ years.

Ms. M. Alekhya currently Pursuing B.Tech in the department of E.C.E from Gayatri Vidya Parishad College of Engineering for Women, Visakhapatnam.

Ms. P. Sahithi currently Pursuing B.Tech in the department of E.C.E from Gayatri Vidya Parishad College of Engineering for Women, Visakhapatnam.

Ms. K. Sireesha currently Pursuing B.Tech in the department of E.C.E from Gayatri Vidya Parishad College of Engineering for Women, Visakhapatnam.