International Journal of Modern Electronics and Communication Engineering (IJMECE) ISSN: 2321-2152
Volume No.-7, Issue No.-4, July, 2019

Design of a Voltage Reference Circuit

Dr. Jasbir Kaur
ECE Department
Punjab Engineering College (Deemed to be university),
Chandigarh, India
E-mail: jasbirkaur70@yahoo.co.in

Shivani
ECE Department
Punjab Engineering College (Deemed to be university),
Chandigarh, India
E-mail: shivani2053@gmail.com

Abstract: This paper describes the design of a reference voltage, implemented using 180nm CMOS technology. Firstly, the design has been made using a simple current mirror. This circuit generates a reference voltage of 1.1948V. It can operate between -40°C to 125°C. Total variation of reference voltage within this temperature range is 0.62mV which is 0.05189% of the reference voltage. Secondly, the circuit is made using a better current mirror, i.e. a cascode current mirror for better matching purpose. This circuit generates a reference voltage of 1.10857V. It can also operate between -40°C to 125°C. Finally, the variation of the reference voltage with the variation of supply voltage is analyzed.

Keywords: Reference voltage, Current mirror, Cascode current mirror, CMOS, CTAT and PTAT.

I. INTRODUCTION

Voltage reference is the major building block for a variety of analog and mixed signal electronic devices such as data converters viz. Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs), Pulse Width Modulator (PWMs), oscillators, controllers, linear regulators, Phase Locked Loops (PLLs), etc. Bandgap Voltage Reference circuit produces a voltage which is less variant with respect to supply variations and temperature variations.

Bandgap reference can be implemented using both Bipolar and CMOS technologies. The principle of the bandgap circuit depends on two groups of diode-connected BJT transistors operating at different emitter current densities. The positive temperature coefficient of the PTAT (Proportional-To-Absolute-Temperature) circuit is cancelled with the negative temperature coefficient of the PN junction diode and a fixed DC voltage is generated which does not vary with temperature. The resulting voltage is about 1.2–1.3 V (depending on the specific technology used) which is quite close to the theoretical band gap of silicon at 0K [1].

Usually, a bandgap reference circuit comprises of a self biasing circuit, a diode connected BJT transistor generating CTAT voltage (a voltage with negative temperature dependence), a PTAT circuit and a feedback mechanism to improve the performance. Current mirrors with current feedback mechanism are used to minimize the supply dependence on the output reference voltage. The circuit can be optimized for minimum temperature and supply dependence with simple modifications the circuit.

A. Bandgap Voltage Reference

In a circuit, there are some currents or voltages which are Proportional-To-Absolute-Temperature (PTAT) and some are Complementary-To-Absolute-Temperature (CTAT). So these voltages are adjusted and added in such a manner that they cancel each other in order to generate an almost constant voltage with respect to temperature and supply variations [2].

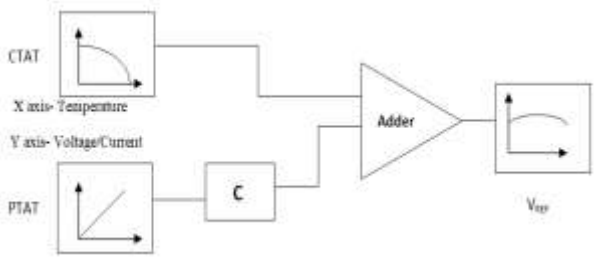


Figure 1: Block diagram of the bandgap reference

II. CIRCUIT DESCRIPTION

A. CTAT and PTAT voltage generation circuit:

Firstly, the circuit for CTAT voltage generation is made and analyzed using Cadence.

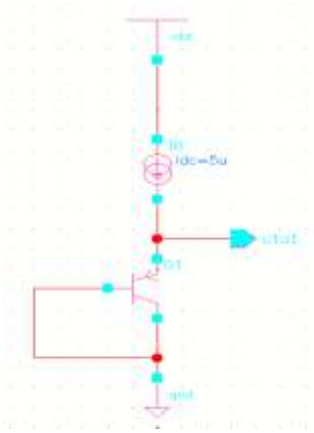


Figure 2: CTAT schematic

The basic equation of diode current is given by

$$I_O = I_S e^{V_D/V_T}$$

Where V_T is the thermal voltage = 26mV /300K, and V_D is the voltage across the diode.

$$V_D = V_T . ln\left(\frac{I_O}{I_S}\right)$$

Since,

$$V_T = \frac{kT}{q}$$

It implies that the thermal voltage of diode is linearly proportional to temperature, i.e.,

$$V_T \propto T$$

Thus, V_T is a PTAT voltage and $ln\left(\frac{I_O}{I_S}\right)$ is a CTAT voltage. But V_T (PTAT) is very weak and CTAT here is very strong. So, effective nature of V_D here is CTAT.

The equation of slope of the CTAT (when I_O is considered constant) is given by

$$\frac{\partial V_D}{\partial T} = \frac{V_D - (4+m)V_T - \frac{E_g}{q}}{T}$$

In order to extract V_T and cancel the term $ln\left(\frac{I_O}{I_S}\right)$ somehow, some voltage (say V_{D1}) has to be subtracted from V_D. For this, let us consider a circuit in Figure 3 [3].

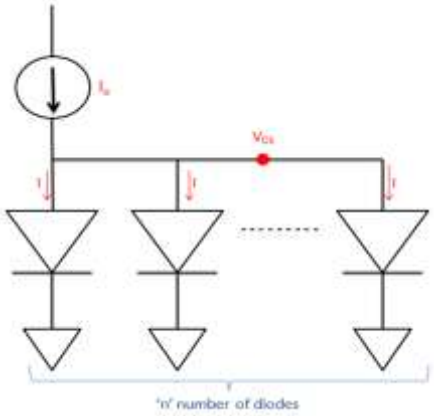


Figure 3: Conceptual generation of PTAT voltage

$$I_O = n.I$$

$$I_O = n.I_S e^{V_{D1}/V_T}$$

$$V_{D1} = V_T . ln\left(\frac{I_O}{n.I_S}\right)$$

It implies, $V_D - V_{D1} = V_T . \ln(n)$

This equation signifies that $V_D - V_{D1}$ is a PTAT.

B. BGR using current mirror:

The generation of PTAT and CTAT voltages is discussed in section II-A. Now, they are combined together in a single schematic using a simple current mirror circuit so that the currents in both the CTAT and PTAT circuit are equal. Moreover, the voltages (VD and V2 in figure 4) are also equal because of current mirror property. The reference voltage should not vary with the supply variation as well. So, 'how good is the current mirror'- decides and confirms that VD=V2 and ultimately rejects the effect of supply variation [3].

MOSFETs NM0, NM1, PM6, PM7, PM8 in the current mirror circuit shown in figure 4 are having same aspect ratios (equal sized MOSFETs), i.e. W=20u and L=5u.

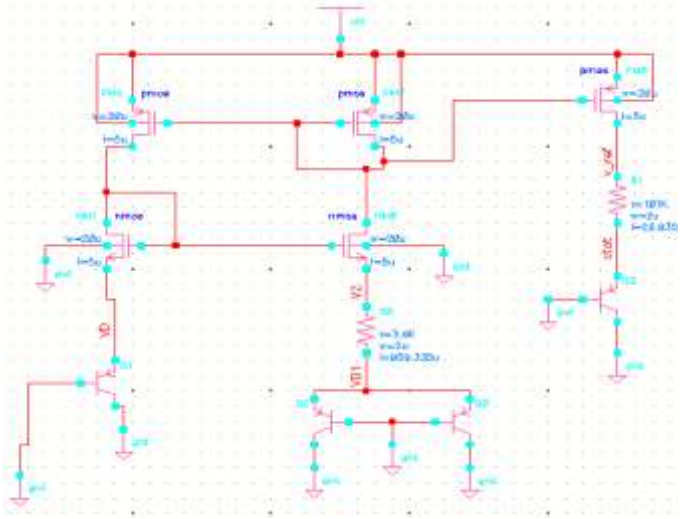


Figure 4: BGR using simple current mirror

The voltage across resistance R0 is a PTAT voltage.

$$I_O R_0 = V_D - V_{D1} = V_T \ln(n)$$

To find the value of resistance R0:

$$I_O R_0 = V_T \ln(n)$$

$$R_0 = \frac{26mV . \ln(2)}{5uA}$$

$$R_0 = 3.6k\Omega$$

The PTAT current is duplicated into another branch using the property of current mirror.

Voltage across resistor R1 is also PTAT voltage and is given by

$$V_{R1} = I_O . R_1 = \frac{R_1}{R_0} . V_T . \ln(n)$$

The CTAT voltage cannot be manually adjusted much. So, the PTAT voltage is adjusted by adjusting the factors 'R_1', 'R_0' and 'n' in such a manner that this PTAT voltage cancels the CTAT voltage and results in an almost constant voltage or a less varying voltage with respect to temperature.

When I_O current is considered as PTAT current, the slope of CTAT voltage is given by:

$$\frac{\partial V_D}{\partial T} = \frac{V_D - (3+m)V_T - \frac{E_g}{q}}{T}$$

The cascode current mirror is a better current mirror circuit. So, it can be used for better matching and for better supply rejection purposes.

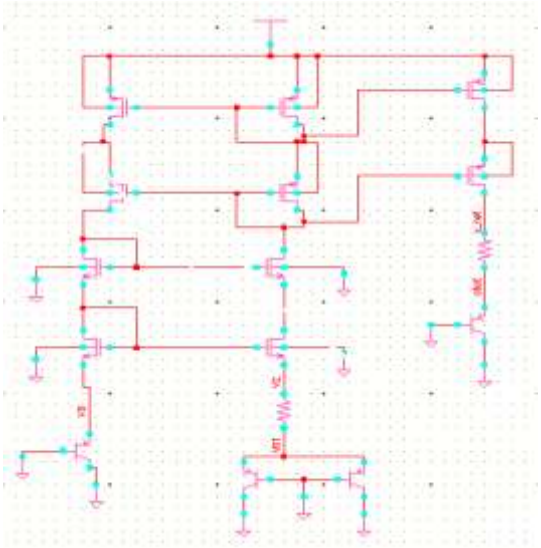


Figure 5: BGR using cascode current mirror

If I_O is considered as 5uA and n=2, then R1=97.74kΩ. It is an approximate calculated value.

III. SIMULATION AND RESULTS

The CTAT schematic in figure 2 is simulated and its DC response with varying temperature range from -40°C to 125°C is analyzed and the negative temperature dependence of CTAT voltage is observed.

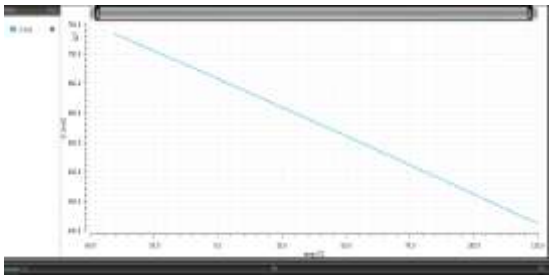


Figure 6: DC response of CTAT schematic

Figure 7 shows the DC response of CTAT and PTAT voltages with temperature sweeping between -40°C to 125°C. The slopes of PTAT and CTAT are also plotted and analyzed.

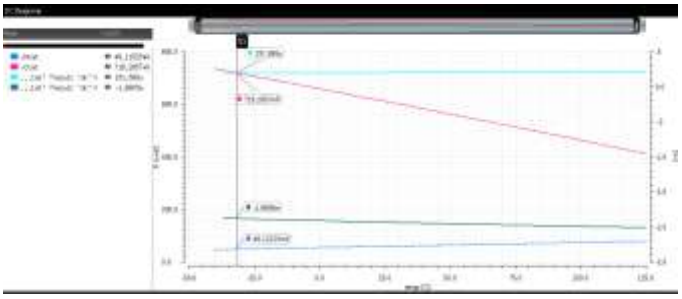


Figure 7: PTAT and CTAT plot along with their respective slopes

For the voltage VD to be equal to V2, the current in both the branches has to be approximately equal. So, the current analysis of BGR made using current mirror is done so as to make sure that the current in both branches is equal and the current mirror is working properly.

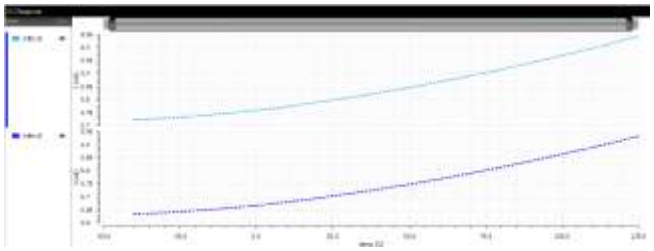


Figure 8: Current analysis in BGR

Figure 9 shows the voltage VD and V2 responses that they are almost equal.

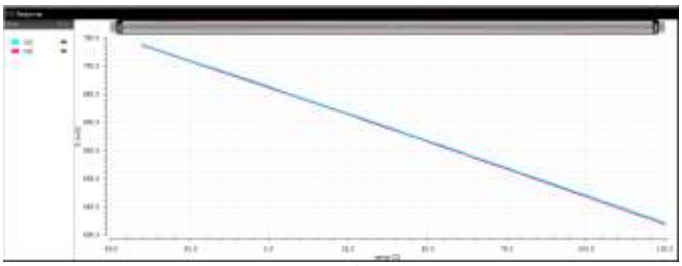


Figure 9: DC response of voltages VD and V2

BGR using simple current mirror has been simulated with R1=10kΩ, the PTAT voltage across resistor R1 varies from 46.5mV to 78mV (approx) and the PTAT_2 voltage across resistor R0 varies from 16mV to 27mV.

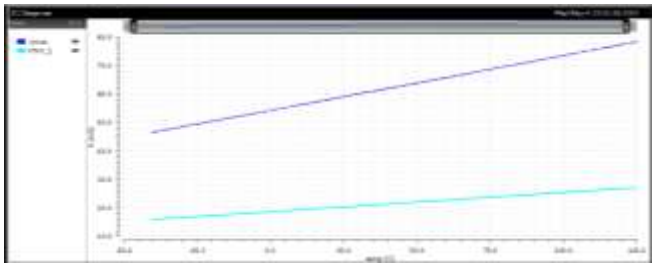
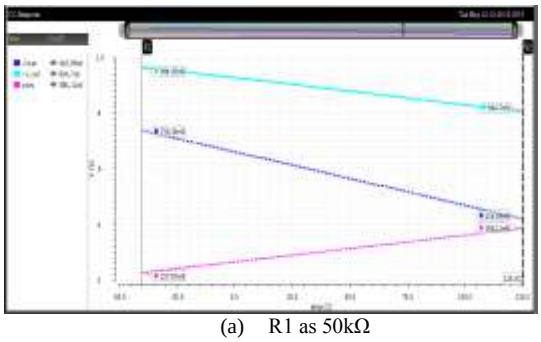
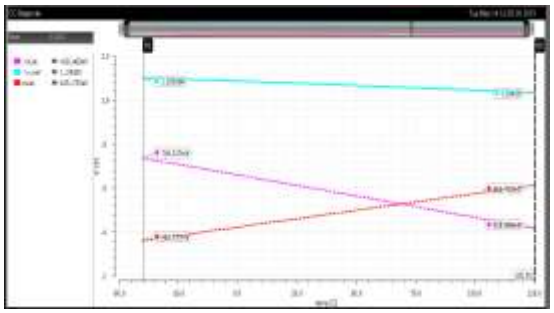


Figure 10: PTAT across R0 and PTAT across R1 response

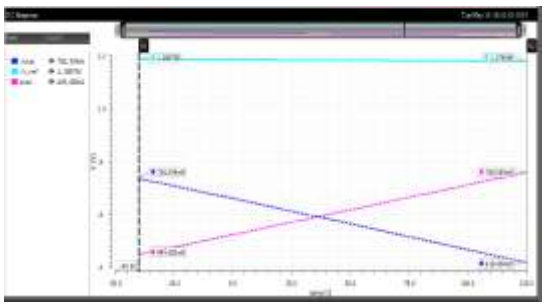
Figure 11 shows the plots of reference voltage for different values of resistance R1. It can seen that the reference voltage is least variant for R1=101kΩ. Total variation of reference voltage within the temperature range -40°C to 125°C for R1=101kΩ is 0.62mV which is 0.05189% of the reference voltage.



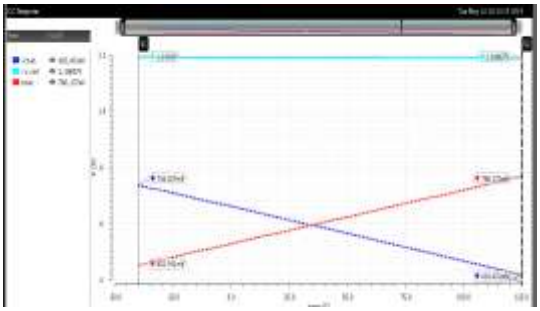
(a) R1 as 50kΩ



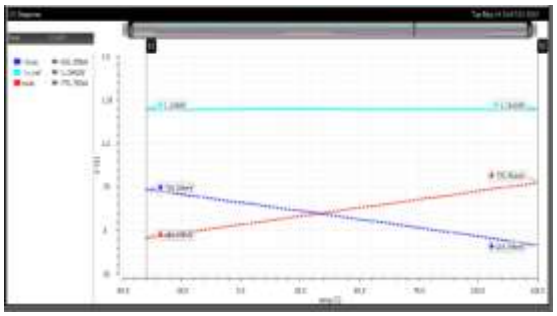
(b) R1 as 80kΩ



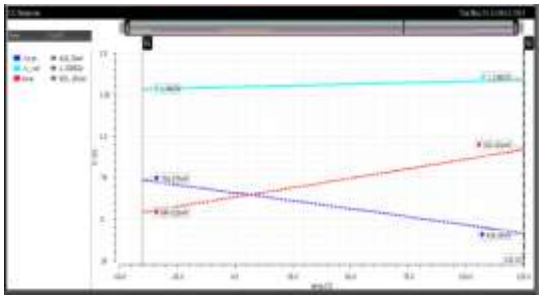
(c) R1 as 99kΩ



(d) R1 as 100kΩ



(e) R1 as 101kΩ



(f) R1 as 120kΩ

Figure 11 (a)-(f): Reference voltage, PTAT and CTAT voltages for different values of R1

Figure 12 shows the DC response of reference voltage with supply variation. It can be observed that

V_{REF}=1.008V for V_{DD}=1.421V

V_{REF}=1.313V for V_{DD}=4.396V

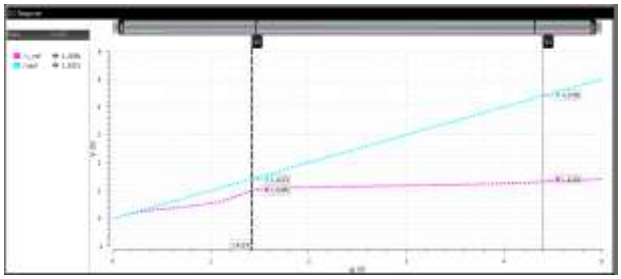


Figure 12: DC response of reference voltage of BGR using simple current mirror with supply variation

For better matching, better current mirror has to be used because current mirror is responsible for supply rejection. Thus, BGR using cascode current mirror is simulated and figure 13 shows the DC response of reference voltage with respect to supply variation.

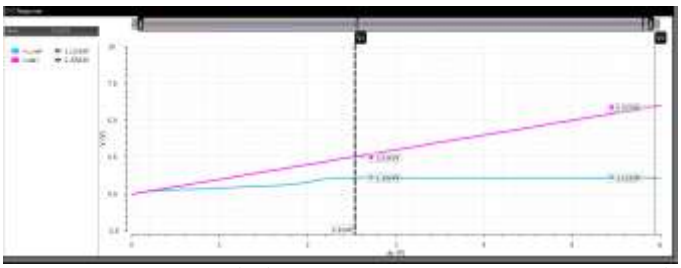


Figure 13: DC response of reference voltage with supply variation in case of cascade current mirror BGR

It can be observed that:

V_{REF}=1.1014V for V_{DD}=2.5343V

V_{REF}=1.1123V for V_{DD}=5.9379V

Table 1: Comparison between BGR using simple current mirror circuit and BGR using cascode current mirror circuit with respect to supply variations

Sr. No.	Supply voltage (in Volts)	V_{REF} for BGR using cascode current mirror circuit (in Volts)	V_{REF} for BGR using simple current mirror circuit (in Volts)
1.	2.188	1	1.129
2.	2.993	1.109	1.175
3.	3.8	1.109	1.239
4.	4.549	1.109	1.335
5.	4.91	1.109	1.401
6.	5	1.109	1.417

This clearly implies that cascode current mirror performs better than simple current mirror for supply rejection purpose in BGR.

IV. CONCLUSION

The design methodologies of bandgap voltage reference circuit have been discussed. The focus of this paper is mainly on

the generation of PTAT and CTAT voltages and design of the BGR circuit using current mirror circuit. Since, different types of current mirrors are available, so the circuit is designed using a simple current mirror and a cascode current mirror and the result is analyzed and compared.

It can be concluded that for the better matching purpose, a better current mirror has to be used because the current mirror is responsible for the supply rejection in bandgap voltage reference circuit.

Apart from this, it can be observed and concluded that the reference voltage in case of BGR using cascode current mirror does not reach 1.2V at anytime. It is because of the voltage drop across all the four MOSFETs. So, in case of Cascode current mirror BGR, a higher minimum supply voltage is needed.

REFERENCES

[1] Baker, R.J., 2019. CMOS: circuit design, layout, and simulation. Wiley-IEEE press.

[2] Mok, P.K. and Leung, K.N., 2004, October. Design considerations of recent advanced low-voltage low-temperature-coefficient CMOS bandgap voltage reference. In Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004 (pp. 635-642). IEEE.

[3] Razavi, B., 2005. Design of analog CMOS integrated circuits.

[4] Leung, K.N., Mok, P.K. and Leung, C.Y.A., 2-V 23-uA 5.3-ppm/". C Curvature Compensated CMOS Bandgap Voltage Reference', IEEE Journal of Solid-State Circuits,38(3) , pp.561-564.

[5] Parisi, A., Finocchiaro, A. and Palmisano, G., 2017. An accurate 1-V threshold voltage reference for ultra-low power applications. Microelectronics Journal, 63, pp.155-159.

[6] Wu, W., Zhiping, W. and Yongxue, Z., 2007, December. An improved CMOS bandgap reference with self-biased cascoded current mirrors. In 2007 IEEE Conference on Electron Devices and Solid-State Circuits (pp. 945-948). IEEE.

[7] Xing, X., Wang, Z. and Li, D., 2007, November. A low voltage high precision CMOS bandgap reference. In Norchip, 2007(pp. 1-4). IEEE.

[8] Zeki, A. and Kuntman, H., 1997. Accurate and high output impedance current mirror suitable for CMOS current output stages. Electronics Letters, 33(12), pp.1042-1043.

AUTHOR'S BIOGRAPHIES

Dr. Jasbir Kaur is an Assistant Professor in Punjab Engineering College (Deemed to be University), Chandigarh since 2000. Her area of research interests includes VLSI design and Communication.

Shivani is pursuing M.Tech in Electronics (VLSI Design) from Punjab Engineering College (Deemed to be University), Chandigarh. Her current research work includes CMOS op-amp and current mirror design and Bandgap voltage reference design for analog applications.