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Design of low power, mixed logic 2x4 decoders using FinFET

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Abstract: This paper presents the design of 2x4 decoders using mixed -logic design methodology which combines the transmission gate logic and pass transistor logic with the static CMOS using FinFET. FinFET's have emerged as the successor to the MOSFET technology because of the increased leakage current and various short channel effects that limits the use of MOSFET at deeply scaled technology nodes. Two circuits for the decoder are presented here: a 14 transistor circuit for reduction of transistor count and power dissipation and a 15 transistor circuit for high power delay performance. Decoders are designed using both MOSFET and FinFET technologies and the results (power dissipation, delay) are compared. 32nm technology is chosen for the circuits and the simulations are done using HSpice software..

Keywords: MosFet, Pass-transistor, Transmission-gate, FinFet, Mixed–logic, Decoder

I. INTRODUCTION

Static CMOS circuits are used in majority of the logic gates in Integrated circuits [1]. CMOS logic offers good performance, resistance to noise, robustness against voltage scaling and transistor sizing. Pass transistors and Transmission gates are used to make different logic circuits as they reduce the transistor count by eliminating redundant gates. Reduced transistor count leads to reduction in area, power and delay in the circuit [2-4]. Pass transistor circuit can be easily implemented using either the individual nMos/pMos pass transistors or by the parallel connection of nMos and pMos called as transmission gates.

Continual scaling of the MOSFET has led to the increase in the transistor density and performance of the Integrated circuits. However, further scaling in the nanometer range has also given rise to various problems like increase in leakage current (I_{off}), increase in power dissipation, V_{Th} roll-off, interconnect capacitance etc. Short channel effects degrade the performance and eventually limit the scaling [5,6].

To tackle with these short channel effects, a new device called FinFET [7,8] is now being used as an alternate to the MOSFET. It has been shown that FinFET have helped reducing the short channel effects. Multiple-gate field-effect transistors (MGFETs) or FinFET exhibit better screening of the drain potential from the channel because of the vicinity of the additional gate(s) to the channel and thus the higher gate channel capacitance. This makes them superior to MOSFETs in short channel performance metrics, such as subthreshold slope (*S*), drain-induced barrier lowering (DIBL), and threshold voltage (V_{Th}) roll-off, I_{off}. Improvement in these metrics implies less degradation in the transistor's *V*th with continued scaling, which in turn implies less degradation in Ioff [9-12].

Section II of the paper gives the overview of the decoder circuit. Section III discuss the two mixed logic designs of the decoder circuit [13] and finally section IV and V have the results and the conclusion respectively.

II. OVERVIEW OF DECODER CIRCUITS

In digital electronic system, information is represented using binary codes ('0', '1'). For an n-bit binary code, 2^n distinct elements of coded data can be represented.

A decoder is a combinational circuit which is used to convert a binary code into set of signals. It has 'n' input lines and maximum of 2^n output lines. One of these output will be active high based on combination of input bits, when decoder is enabled i.e. decoder detects a particular code.

2x4 Decoder

A 2x4 decoder generates 4 min-terms Y_{0-3} for 2 input variables A, B. Depending upon the input combination, one of the 4 output lines is selected and is set high ('1') and rest of the output lines are set to low ('0') as shown in table 1.

Table 1: Truth table of 2x4 Decoder

A	B	Y_0	Y_1	Y_2	Y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

A 2x4 decoder can be implemented using 4 NOR gates and 2 Inverters which adds up to 20 transistors as shown in Fig.1.

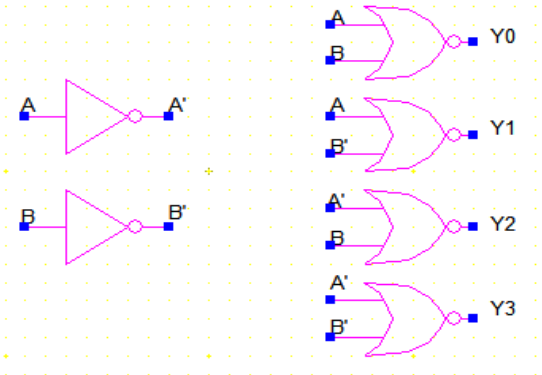

Figure 1. 20 transistor 2x4 decoder.

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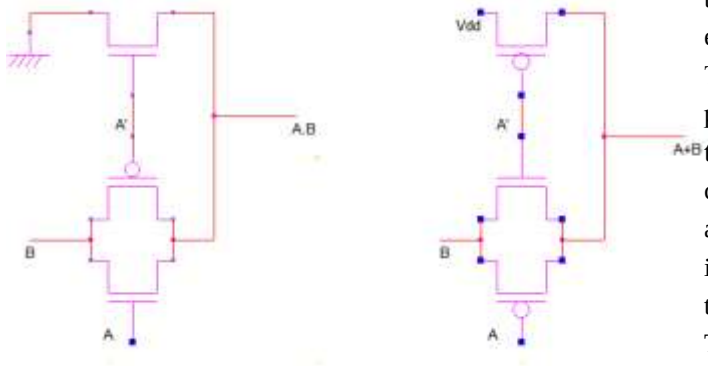
III. MIXED LOGIC DESIGNS

Transmission gates are mostly used in circuits which are based on XOR logic e.g. adders and also used in multiplexers as switch elements. They can also be used to implement AND/OR logic as demonstrated in [14], which can be used in decoder. The 2 input transmission gate logic AND/OR circuits are shown in Fig.2.

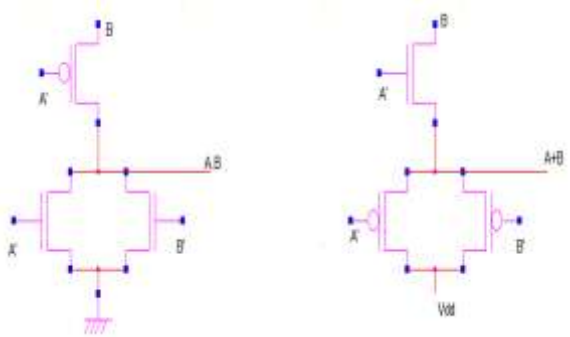


(a) (b)

Figure 2. Three transistor TGL AND/OR gates used in decoder. (a) TGL AND gate (b) TGL OR gate

In TGL circuits, input A is controlling the gate terminals of all the 3 transistors and input B propagates through the transmission gate.

In Pass transistor logic we consider DVL style in which both nMOS and pMOS transistors are used. DVL offers advantage upon DPL style, preserving its full swing operation with reduced transistor count [15]. The 2 input DVL logic AND/OR circuits are shown in Fig.3.



(a) (b)

Figure 3. Three transistor DVL AND/OR gates used in decoder (a) DVL AND gate (b) DVL OR gate

In DVL logic, input A controls the gate terminals of 2 transistors while input B controls gate terminal of 1 gate and propagates through a pass transistor to the output.

In Fig. 2 and Fig. 3 above we saw that TGL/DVL gates require only 3 transistors as opposed to the 4 transistors required by the CMOS NOR gate for the implementation of decoder. Thus, resulting in reduced transistor count.

A. 14-transistor Low-Power 2x4 decoder.

Designing the decoder using TGL/DVL logic requires a total of 16 transistors by using proper signal arrangement which eliminates the use of one inverter circuit.

To eliminate the 'B' inverter from the circuit, we use 'A' as propagation signal and 'B' as controlling signal in DVL part of the circuit and we use 'B' as the propagation signal and 'A' as controlling signal in TGL part of the circuit. Similarly, we can also eliminate the A inverter from the circuit instead of the B inverter. This elimination of any one inverter reduces the transistor count of the 2x4 decoder to 14.

The inverter elimination reduces the transistor count, logical effort and overall switching activity of the circuits, thereby minimizing power dissipation. Fig. 4 shows the 14 transistor 2x4 Decoder circuit [13].

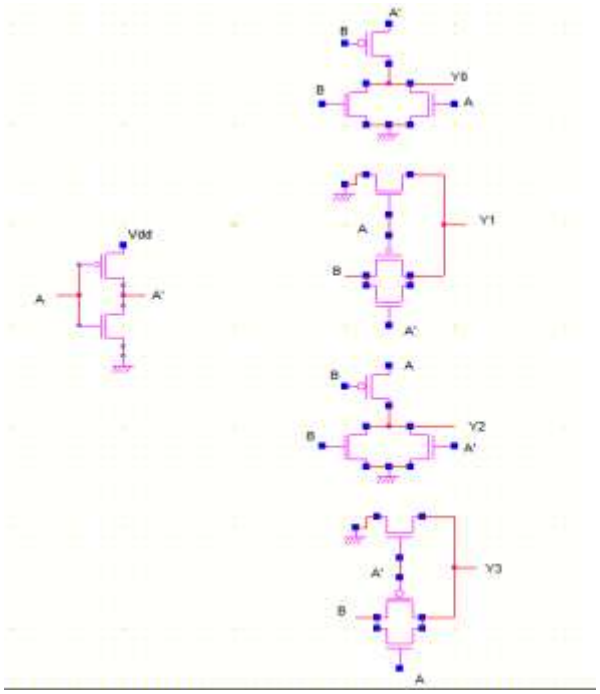


Figure 4. 14 transistor circuit for 2x4 Decoder

B. 15-transistor High-Performance 2x4 decoder.

In 14 transistor topology we can observe that there is a drawback regarding the worst case delay because of the use of complimentary A as the propagation signal in realizing Y0. Y0 can be more efficiently realized using the simple NOR gate circuit and eliminate the use of complimentary signal.

This use of NOR gate for realizing Y0 adds one more transistor in the circuit but it improves the delay performance as A will propagate directly rather than propagating through an inverter. There is a slight increase in power dissipation because of

addition of an extra transistor. Fig. 5 shows the 15 transistor 2x4 Decoder circuit [13].

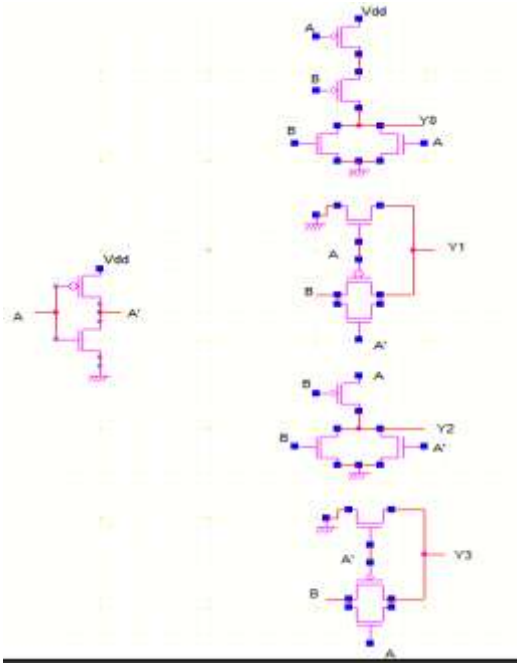


Figure 5. 15 transistor circuit for 2x4 Decoder

IV. SIMULATION AND RESULT

Mixed logic 2x4 decoders are implemented using MOSFET and FinFET at 32nm and their results (power dissipation, delay) are shown in this section.

Device parameters used for MOSFET technology:
L (Channel length) =32nm
W_P (PMOS width) = W_N (NMOS width) = 64nm
AS (Source area) = 2.25p
PS (Source perimeter) = 6.8u
AD (Drain area) = 2.25p
PD (Drain perimeter) = 6.8u

Device parameters used for FinFET technology:
L (Channel length) =32n
HFIN (Fin height) = 10n
TFIN (Fin thickness) = 10n
NFIN = 2
NRS (square of source diffusion) = 1
NRD (square of drain diffusion) = 1

Results for 2x4 decoder implemented using MOSFET and FinFET using above parameters are shown here. The results are calculated for both 14 transistor low-power design and 15 transistor high-performance design. All the simulations are done in HSPICE and AWAVES.

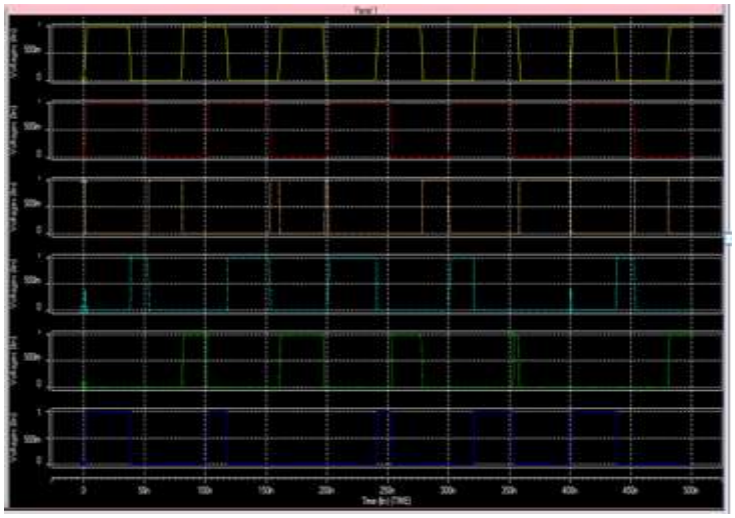


Figure 6: Output waveform for 2x4 decoder circuit.

Power dissipation, delay are shown in table 2 and comparison is shown in figure 7 & 8 respectively.

Table 2: Result comparison of decoder using MOSFET and FinFET technologies

	Power dissipation (W)		Delay (s)	
Technology	14 Transistor	15 Transistor	14 Transistor	15 Transistor
MOSFET	**4.30E-07**	**4.40E-07**	**4.41E-08**	**4.34E-08**
FinFET	**1.86E-08**	**2.10E-08**	**2.79E-08**	**2.71E-08**

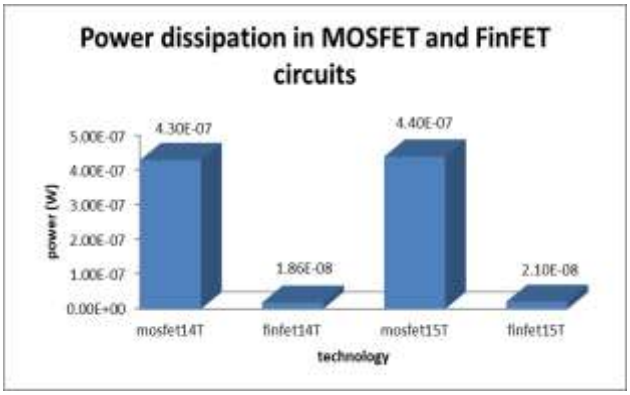


Figure 7: Power dissipation comparison

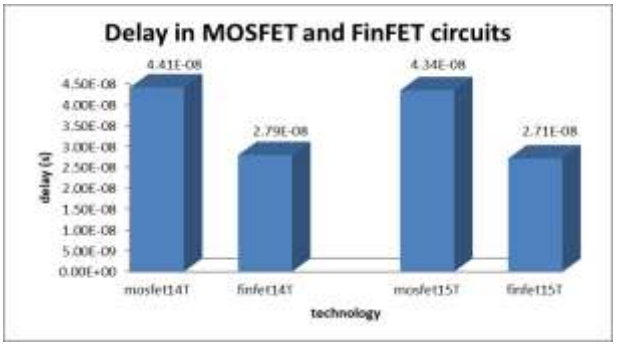


Figure 8: Delay comparison

- Through the result obtained by simulations in HSPICE software we can see that there is a significant reduction in power dissipation and delay by using FinFET technology.
- In 14 transistor circuit, power dissipation is almost reduced by a factor of '23' in FinFET circuit as compared to the MOSFET circuit and delay is reduced by a factor of '1.6'.
- In 15 transistor circuit, power dissipation is almost reduced by a factor of '21' in FinFET circuit as compared to the MOSFET circuit and delay is reduced by a factor of '1.6'.
- Also, we can see that the 14 transistor circuit of the decoder dissipates less power than its 15 transistor counterpart but the 15 transistor circuit is slightly better than 14 transistor circuit in terms of delay in both MOSFET and FinFET technologies.

REFERENCES

[1] N. H. E. Weste, D. M. Harris, CMOS VLSI Design a Circuits and Systems Perspective, Boston, MA, USA:Addison-Wesley, 2011.

[2] R. Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic", IEEE J. Solid State Circuits, vol. 32, no. 7, pp. 1079-1090, Jul. 1997.

[3] K. Yano et al., " A 3.8-ns CMOS 16x16-b multiplier using complementary pass-transistor logic ", IEEE J. Solid-State Circuits, vol. 25, no. 2, pp. 388-393, Apr. 1990.

[4] V. G. Oklobdzija, B. Duchene, "Pass-transistor dual value logic for low-power CMOS", Proc. Int. Symp. VLSI Technol., pp. 341-344, 1995.

[5] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," Proceedings of the IEEE, vol. 89,no. 3, pp. 259–288, 2001.

[6] K. J. Kuhn, "CMOS scaling for the 22nm node and beyond: Device physics and technology," in Proceedings of the International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA '11), pp. 1–2, April 2011.

[7] Hisamoto, D., Lee, W.C., Kedzierski, J., Takeuchi, H., Asano, K., Kuo, C., Anderson, E., King, T.J., Bokor, J. and Hu, C., 2000. FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. IEEE Transactions on Electron Devices, 47(12), pp.2320-2325.

[8] Bhattacharya, D. and Jha, N.K., 2014. FinFETs: From devices to architectures. Advances in Electronics, 2014.

[9] Nowak, E.J., Aller, I., Ludwig, T., Kim, K., Joshi, R.V., Chuang, C.T., Bernstein, K. and Puri, R., 2004. Turning silicon on its edge [double gate CMOS/FinFET technology]. IEEE Circuits and Devices Magazine, 20(1), pp.20-31.

[10] "International technology roadmap for semiconductors," 2011, http://www.itrs.net.

[11] Veshala, M., Jatooth, R. and Reddy, K.R., 2013. Reduction of short-channel effects in FinFET. International Journal of Engineering and Innovative Technology (IJEIT), 2(9), pp.118-124.

[12] Prasad, M. and Mahadevaswamy, U.B., 2017. Comparative Study of MOSFET CMOS and FINFET: A Review. In Third International Conference on Current Trends in Engineering Science and Technology ICCTEST-2017.

[13] Balobas, D. and Konofaos, N., 2016. Design of low-power high-performance 2–4 and 4–16 mixed-logic line decoders. IEEE Transactions on Circuits and Systems II: Express Briefs, 64(2), pp.176-180.

[14] X. Wu, "Theory of transmission switches and its application to design of CMOS digital circuits", Int. J. Circuit Theory Appl., vol. 20, no. 4, pp. 349-356, 1992.

[15] D. Marković, B. Nikolić, V. G. Oklobdžija, "A general method in synthesis of pass-transistor circuits", Microelectron. J., vol. 31, pp. 991-998, 2000.