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Low Power 4-Bit Arithmetic Logic Unit Using Full-Swing GDI Technique

N Kiran Kumar[1]
Assistant Professor
ECE Department
Vemu Institute of Technology
P Kotha kota, Andhra Pradesh, India.
kirankumarece@vemu.org

ABSTRACT-Power dissipation and space of the circuit area unit the most problems within the industry, this paper provides a style of 4-Bit Arithmetic Logic Unit (ALU) exploitation Full-Swing GDI Technique, that thought of a good technique for low power digital style whereas reducing the realm of the circuit compared to alternative logic designs. The projected ALU style consists of 2x exploitation 65nm TSMC method. The results show that the projected style consume less power exploitation less range of transistors, whereas achieving full swing operation compared to previous work

I. INTRODUCTION

In our daily life, we use a lot of portable electronic devices; these devices basically are low power high speed VLSI circuits works simultaneously. One of these circuits is the Arithmetic logic unit (ALU) which considered an essential component in many applications such as Microprocessor, digital signal processing, image processing, etc.

Addition considered essential part of the arithmetic unit and almost all other arithmetic operations includes addition therefore any improvement in the adder cell is reflected as a major improvement in the ALU. In this paper a 4-Bit ALU is designed using a low power adder cell realized by the Full-Swing GDI technique and compared to previous work in terms of power dissipation and transistor count. Simulation environment is cadence virtuoso using TSMC 65nm process.

II. LITERATURE SURVEY

[1] A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, and A. Fish, "Fullswing gate diffusion input logic—Case-study of low-power CLA adder design," Integration, the VLSI Journal, vol. 47, no. 1, pp. 62–70, Jan. 2014.

Power consumption and area reduction of logic and memory have become primary focuses of attention in VLSI digital design. Power is the limiting factor in both high performance systems and portable applications. Die area directly affects the device size and cost. Since the introduction of the standard CMOS Logic in early 80s, many design solutions have been proposed to improve power dissipation, area and performance of digital VLSI chips. Gate Diffusion Input (GDI) design methodology was introduced as a promising alternative to Static CMOS Logic.

[2] M. Shoba, R. Nakkeeran, "GDI based full adders for energy efficient arithmetic applications", Engineering Science and Technology, an International Journal, vol. 19, no. 1, pp. 485–496, Mar. 2016.

Power delay product or energy consumption per operation has been introduced to accomplish optimal design tradeoffs. The performance of digital circuits can be optimized by proper selection of logic styles. Gate Diffusion Input (GDI) is a lowest power design technique which offers improved logic swing and less static power dissipation. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors. In this paper, an efficient methodology for digital circuit such as AND, OR, and XOR gates with full swing is implemented. After that, three full adders are proposed based on the full swing gates in a standard 45 nm technology. Methodology for digital circuit such as AND, OR, and XOR gates with full swing is implemented. After that, three full adders are proposed based on the full swing gates in a standard 45 nm technology.

III. PROPOSED METHOD

GDI Technique was first proposed by Arkadiy Morgenshtein, Idan Shwartz and Alexander Fish this technique allows implementation of various complex logic functions using only two transistors.

However, it was proposed for fabrication in twin-well CMOS or silicon on insulator (SOI) processes, it allowed improvement in power consumption, delay and area of digital circuits compared to CMOS and PTL techniques. The drawback in GDI cell was it suffered from reduced voltage swing due to threshold drops, which leads to performance degradation and increasing static power dissipation. To improve the output of the GDI cells Swing restoration circuits utilized. Morgenshtein et al.Proposed the Modified-GDI approach, shown in Fig (b) where the substrate terminals of NMOS and PMOS transistors connected permanently to GND and VDD, respectively. This modification enables fabrication of GDI cell in standard CMOS processes which is cost efficient compared to twin well and (SOI) processes.

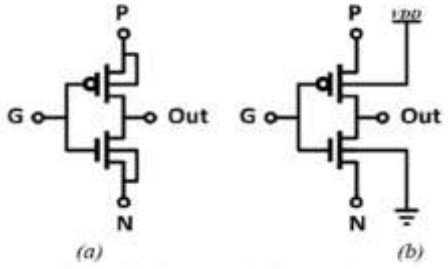


TABLE I DIFFERENT LOGIC FUNCTIONS REALIZATION USING GDI CELL.

N	P	G	OUT	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B$+AC	MUX
0	1	A	$\bar{}$	NOT

In Full-Swing GDI cells proposed as an alternative for swing restoration buffers in this technique, swing restoration transistor utilized to improve the output swing of F1 and F2 gates (universal gates used to realize any logical expression) through this technique full swing operation can be achieved using additional transistors but when compared to CMOS realization it uses less transistors which leads to reduce the area, improve the power and delay of the circuits.

ARITHMETIC LOGIC UNIT

In this the Full-Swing GDI technique is used to realize the circuits required to design the ALU as follows:

A. 2x1 Multiplexer

A multiplexer is a digital switch chooses the output from several inputs based on a select signal, shown in Fig. 2 a 2x1 multiplexer consists of 6 transistors.

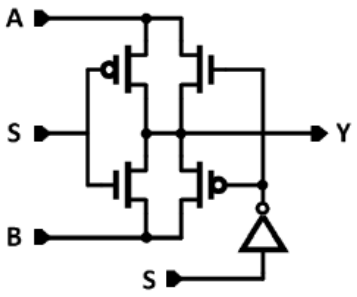


Fig. full swing GDI 2:1 multiplexer

B. 4x1 Multiplexer

Using the previously discussed 2x1 multiplexer a 4x1 multiplexer realized as shown in Fig. consists only of 16 transistors.

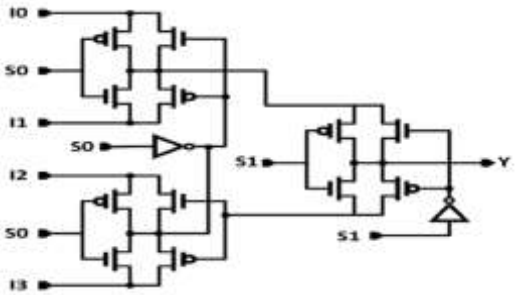


Fig. full swing GDI 4:1 multiplexer

C. Full Adder

A full adder is a combinational circuit that performs the arithmetic sum of three input bits. It consists of three inputs and two outputs. The adder cell used in this design realized using full-swing AND, OR, and XOR gates. This design was chosen among 3 designs to maintain low power operation, it has the lowest delay among the three designs, and with some modifications it performs the logic operations as well, these modifications will save large area of the ALU design.

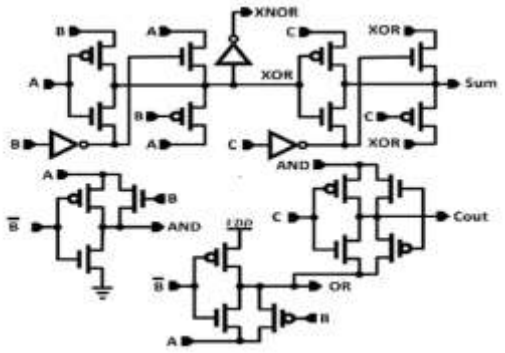


Fig. full-swing full adder cell

D. Design of Arithmetic Logic Unit

An ALU is a key component in the Central Processing Unit (CPU) of any computer; even the simplest microprocessors contain one. It performs arithmetic operations such as addition, subtraction, increment, decrement and logic operations such as AND, OR, XOR and XNOR. The proposed design of the 4-Bit ALU consists of 4 stages, each stage is an 1-Bit ALU realized using the previously discussed circuits as follows: Each 1-Bit ALU stage consists of two 2x1 multiplexers, two 4x1 multiplexers and one full adder cell, this design requires 48 transistors as depicted in Fig. Any desired operation can be performed based on the selection line S0, S1, S2 code; Table II summarizes the truth table of the proposed ALU.

TABLE II. TRUTH TABLE OF THE PROPOSED 4-BIT ALU.

S2	S1	S0	Operations
0	0	0	DECREMENT
0	0	1	ADDITION
0	1	0	SUBSTRACTION
0	1	1	INCREMENT
1	0	0	AND
1	0	1	XOR
1	1	0	XNOR
1	1	1	OR

The 4x1 multiplexer at the input responsible for the B input based on the values of S0 and S1 selection lines it selects from logic 1, B, and logic 0 to perform the Decrement, Addition, Subtraction and the Increment operations respectively, S2 chooses between the arithmetic and the logic operations.

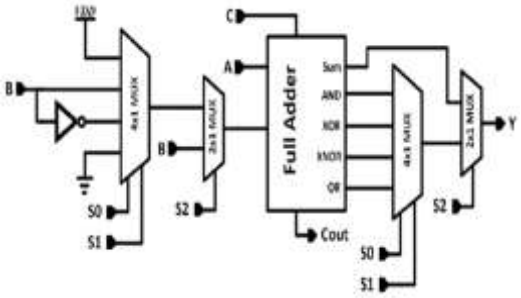


Fig.5.Schematic of 1 bit ALU Stage

To realize the 4-Bit ALU four stages were used as shown in Fig. While the carry input of ALU0 connected to selection line S1 to obtain logic 1 which needed for subtraction and increment operations, however the other values don't affect the results of the logic operations.

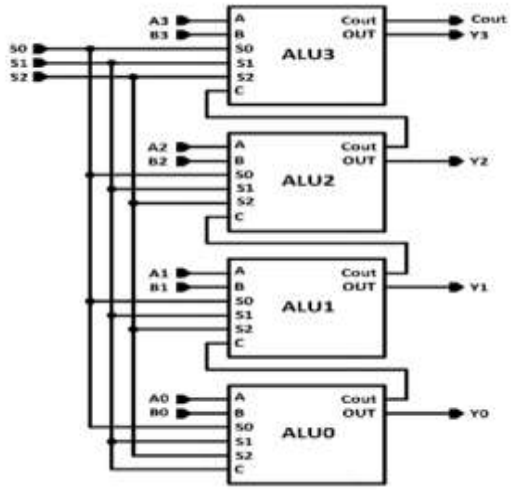
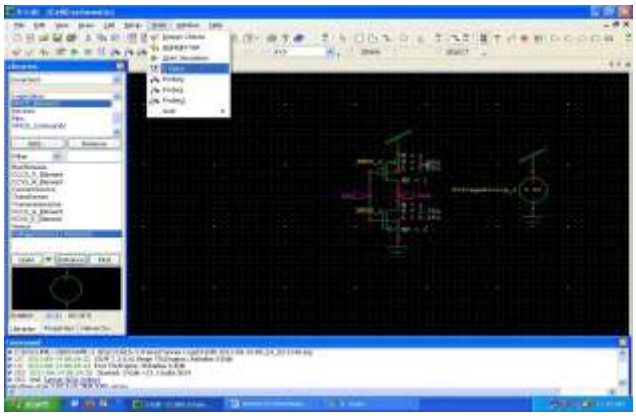


Fig. proposed 4-bit ALU Design

Pre layout simulation

After schematic design you have to check whether your design match with the specification required or not . That's why you need to simulate the design which is called Pre layout simulation.
For simulation go to>> tools>> T-spice>> 'ok



Output of Pre layout simulation of Inverter

IV. CONCLUSION

This work presents a 4-Bit ALU designed in CMOS process using the Full-Swing GDI technique and simulated using the Cadence Virtuoso simulator. Simulation results showed an advantage of the proposed ALU design in terms of power consumption and transistor count, while maintaining Full-Swing Operation. The proposed design consists of 192 transistors and operates under 1V supply voltage.

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