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Efficient FIR Filter design using configurable MAC unit

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Abstract: *The* Low power IC design uses approximate computing and now a day's more attention on this. Few accuracy configurable adder (ACA) designs have been developed to accommodate dynamic levels of approximation but these designs require large area overhead because of carry prediction and redundant computing. If error detection & correction circuitry is included larger area gets increased further. In this paper a simple ACA design without redundancy/correction circuitry is proposed and a very simple carry prediction is used. Here 16 bit adder is designed using simple accuracy reconfigurable adder (SARA) and DAR (delay adaptive reconfiguration) with SARA. Further simple CRA, CLA and SARA is used in Wallace multiplier and Dadda multiplier their area and delay are compared. By these multipliers and adders MAC (multiply and accumulate unit) unit is designed. The MAC unit is mostly demanded in DSP applications. The MAC unit further applied in FIR Filter and compared area and delay for Wallace and Dadda multipliers with adders are compared.

Keywords: ACA, approximate computing, DAR, FIR, MAC, low power design.

I. INTRODUCTION

In advanced VLSI technology power constraints are more important. Low power constraints are already studied. A new one is approximate computing where errors are allowed for power decline. In some applications such as audio, video small errors are allowed. Approximate computing is mainly used in arithmetic circuits. ACA starts with an error detection & correction circuit, it increases the area over head. In this paper carry prediction based configurable adder SARA is proposed. Designing of SARA is simple, occupies less area and delay compared to CRA and CLA.

MAC unit performs both multiply and addition functions. It operates in two stages first it computes the product of numbers and result is forwarded to the second stage addition or accumulate operation. The MAC Units from multiplier circuits. It is used in large number of digital signal processing applications. In this paper, MAC unit is designed with the mentioned adders and multipliers, results are compared in terms of area and delay.

In DSP applications digital filters are mainly used. These are categorizing into 2 types FIR (finite impulse response) and IIR (infinite impulse response) filters. FIR filters are advantageous in terms of stability and linear phase characteristics over IIR filters and these are easy to implement.

In this project FIR filter has been designed using MAC with SARA, CRA and CLA and the results are compared.

II. METHODOLOGIES

ACA design usually classified into 2 categories, error correction based configuration [3][4] & carry prediction based configuration[5]. This design in based on carry prediction based configuration as shown in Fig.1. It starts with accurate adder design which is formed by chaining a set of sub adders. Its sub adders are CRA.

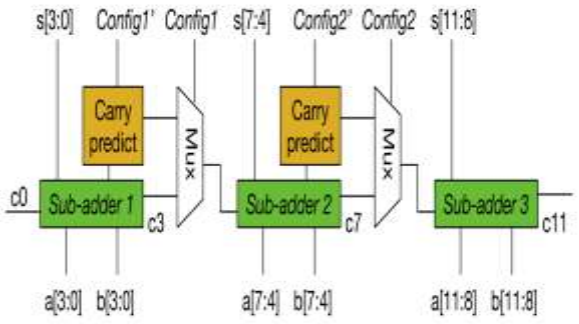


Figure 1. Carry-prediction-based configurable adder type.

A. SARA

In the SARA design M-bit adder is collected of P fragments of H-bit subadders. Here P = [M/H]. Every subadder is similar as CRA excepting that last bit of subadder.

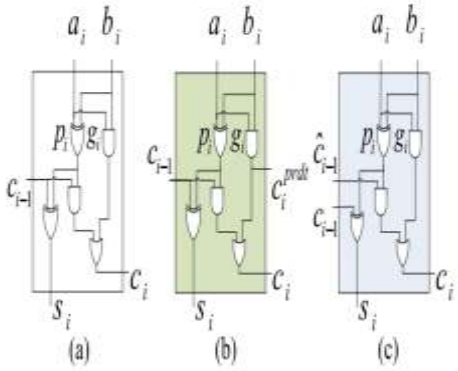


Figure2.(a) full adder. (b) Carry-out full adder.
(c) Carry-in full adder.

An M-bit adder operates on two addends

A= $(a_M, a_{M-1}, \ldots, a_i, \ldots, a_1)$
B= $(b_M, b_{M-1}, \ldots b_i, \ldots b_1)$, for bit i,
Carry input is c_{i-1} &
Carry out is c_i.

Full adder:

$g_i = a_i . b_i$

$p_i = a_i \oplus b_i$

$s_i = p_i \oplus c_{i-1}$

$c_i = g_i + p_i . c_{i-1}$

Carry Out Full adder:

$c_i^{pred} = g_i$

Carry in Full adder:

$s_i = p_i \oplus c_{i-1}$

$c_i = g_i + p_i . \hat{c}_{i-1}$

$$\hat{c}_{i-1} \leftarrow \begin{cases} c_i^{pred}, & \text{if approximate mode} \\ c_i, & \text{if accurate mode} \end{cases}$$

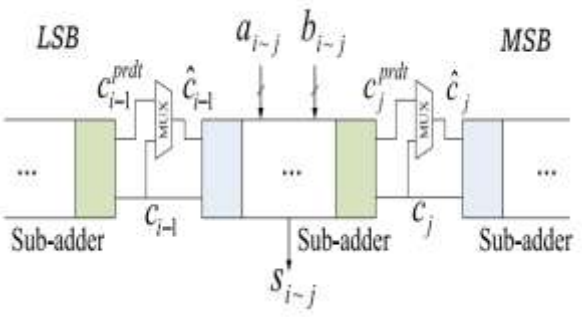
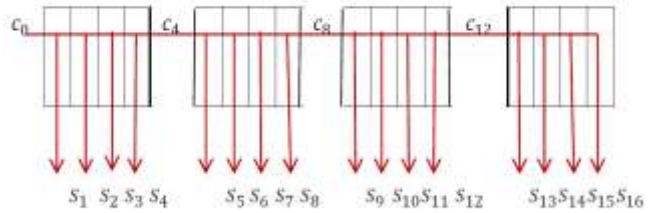


Figure3. Design of SARA.



LSB MSB

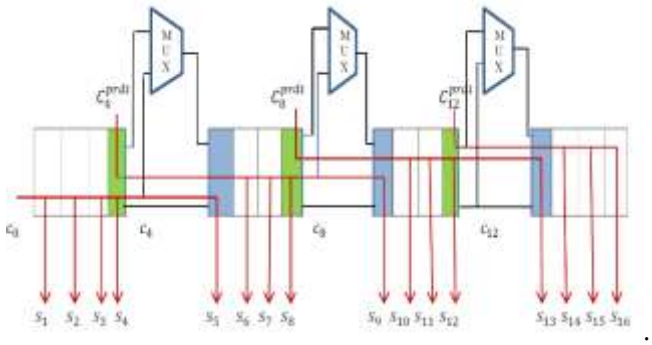


Figure4. Design of 16-bit adder in (a) CRA & (b) SARA.

As show in Fig-4, the 16-bit SARA functioning in approximate mode the sum s_{13} uses the accurate carry c_{12} from a lower subadder (bits 9 to 12).But c_{12} is propagated from approximatecarry c_8^{pred} of another subadder (bits 5 to 8). In SARA s_{13} is has delay up to 9 stages. In RCA, the sum bit s_9 is 12 stages. Comparing these two designs in SARA the delay of sum bit s_{13} is reduced by 6 stages.

B. DELAY-ADAPTIVE RECONFIGURATION OF SARA

The self-configuration is established on the evaluation that the actual worst case path delay depends on added values. The real path delay is huge only when a carry is propagated through a number of consecutive bits. Any incorrect propagation bit from the addends results in a shorter carry propagation chain is short there is no need to use approximate configuration which is planned to cut carry chain shorter. A DAR technique the output of a MUX in SARA is set to approximate mode only a potentially long carry chain is detected the carry chain is short there is no need to go for approximate mode.

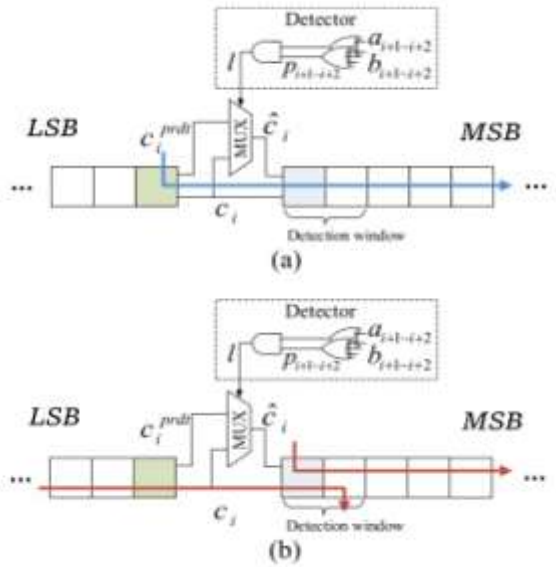


Figure5. Design of DAR of SARA (a) approximate mode & (b) accurate mode

C. *MAC*

The multiplier accumulator [7] operation is used in DSP applications also in multimedia & various other applications. MAC unit has a multiplier adder & accumulator. Here 8 bit Wallace and Dadda multipliers with different adders. The adder is also replaced with SARA, CRA and CLA.

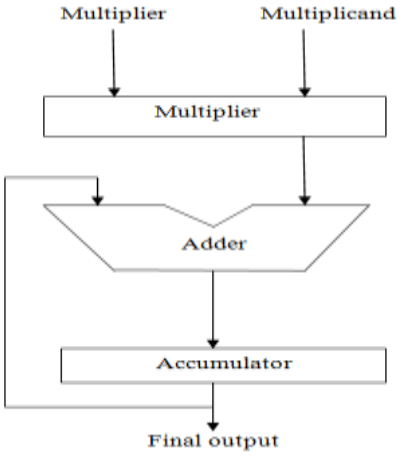


Figure6. MAC Unit

D. *FIR filter*

The basic block for the design and implementation of the DSP processor is the Finite Impulse Response Filter [8]. The FIR filter consists of three basic modules which are adder blocks, flipflops and multiplier blocks. Here 5 tap FIR filter is designed with different adders and compared the area and delay.

Output of the FIR filter is described by this equation

Y[n] = a_0X[n] +a_1X[n-1] +a_2X[n-2] +…..a_{N-1}X[n-N]

X[n] – I/P signal

Y[n] – O/P signal

a_i - Coefficients of the filter

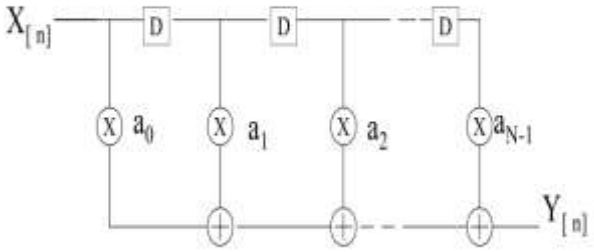


Figure7. FIR filter

III. EXPERIMENTAL RESULTS

In this project the subadder bit-widths of 1, 4, and 8 bits, abbreviated to as SARA1, SARA4 and SARA8 correspondingly.

Table1. 16bit adder comparisons

	Area (LUT's)	Delay (ns)
CRA	53	4.667
CLA	56	3.852
SARA1	31	1.395
SARA4	40	2.816
SARA8	50	3.033
SARA8-DAR2	47	3.847

Table2. FIR filter comparison

	Area (LUT's)	Delay (ns)
FIRMACWALLACECRA	244	7.371
FIRMACWALLACECLA	247	7.363
FIRMACWALLACESARA	205	6.549
FIRMACWALLACECRA	231	7.355
FIRMACWALLACECLA	235	7.344
FIRMACWALACELSARA	184	6.544

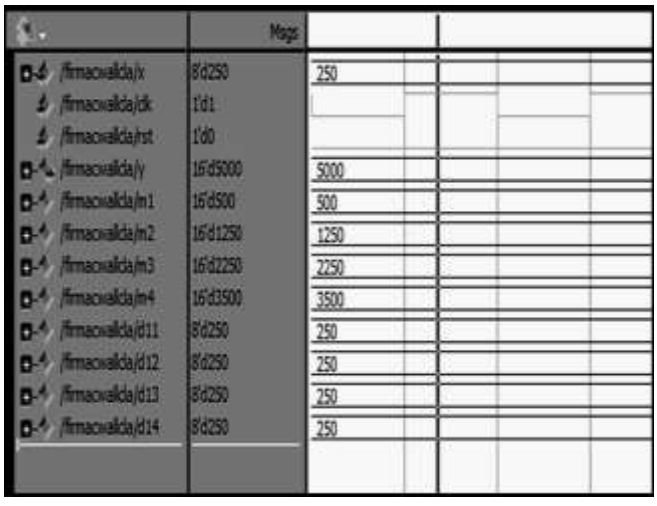


Figure8. FIR filter using MAC with Wallace multiplier & CLA output wave form

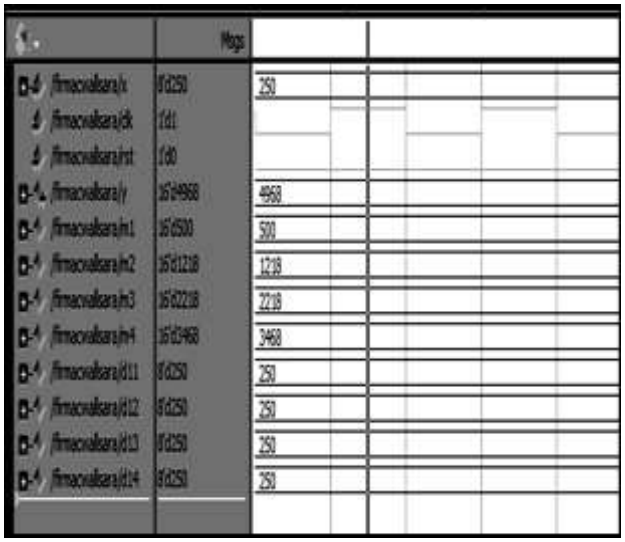


Figure9. FIR filter using MAC with Wallace multiplier and SARA output wave form

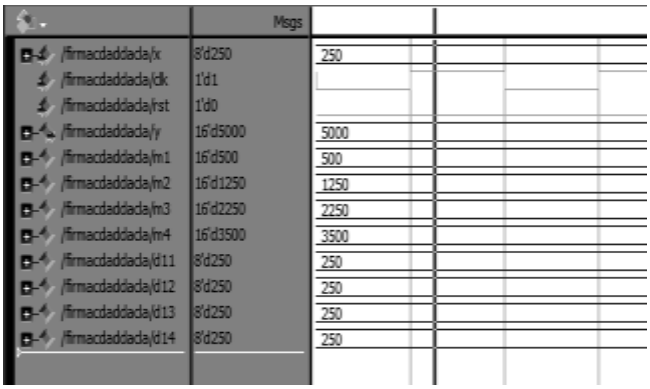


Figure10. FIR filter using MAC with Dadda multiplier & CLA output wave form

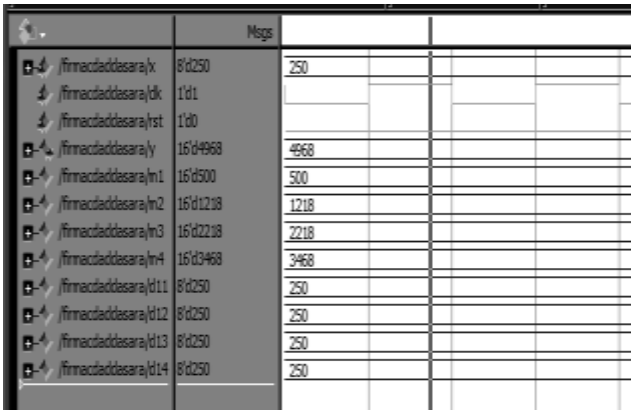


Figure11. FIR filter using MAC with Dadda multiplier & SARA output wave form

IV. CONCLUSION

In this paper SARA and SARA with DAR is designed. SARA significantly reduces the delay and area compared to the latest error correction configurable adder. A Wallace and Dadda Multiplier with SARA are introduced in this paper to increase the performance. The performances of Wallace and Dadda multipliers with CRA, CLA and SARA are compared. A MAC unit with proposed multipliers and reconfigurable adder for digital FIR filter is proposed and its performance is absorved.

REFERENCES

[1] N. Zhu, W. L. Goh, and K. S. Yeo, "An enhanced low-power high-speed adder for error-tolerant application," in Proc. Int. Symp. Integr. Circuits, 2009, pp. 69–72.

[2] J. Han and M. Orshansky, "Approximate computing: An emerging paradigm for energy-efficient design," in Proc. IEEE Eur. Test Symp., May 2013, pp. 1–6.

[3] A. B. Kahng and S. Kang, "Accuracy-configurable adder for approximate arithmetic designs," in Proc. Design Autom. Conf. (DAC), 2012, pp. 820–825.

[4] M. Shafique, W. Ahmad, R. Hafiz, and J.Henkel, "A low latency generic accuracy configurable adder," in Proc. Design Autom. Conf. (DAC), 2015, pp. 1–6.

[5] R. Ye, T. Wang, F. Yuan, R. Kumar, and Q. Xu, "On reconfiguration oriented approximate adder design and its application," in Proc. Int. Conf. Comput.-Aided Design (ICCAD), 2013, pp. 48–54.

[6] S. Venkataramani, K. Roy, and A. Raghunathan,. "Substitute-and simplify: A unified design paradigm for approximate and quality configurable circuits," in Proc. Conf. Design, Autom. Test Eur. (DATE), 2013, pp. 1367–1372

[7] Priyanka nain, Dr. G S virdi, "Multiplier-Accumulator (MAC) Unit", International Journal of Digital Application & Contemporary Research, vol5.2016.

[8] G.J.V.S.N. Lakshmi Devi and M. Ramesh Kumar – "Design and Implementation of Energy Efficient, Reconfigurable Fir filter using Modified Booth and C.S.A.", Journal of Electrical and Electronics Engineering (JEEE), ISSN: 2250-2424, Vol. 2, Issue 1, Sept 2012 11-18.