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Low Power Analog Circuit Design using Memristors

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Abstract: The SR (Set-Reset) flip-flop is one among the simplest circuits which stores 1-bit memory. There are quiet many application of a SR flip-flop. Since memristors can show non-volatile behaviour, it can be used in memory devices. In this paper, SR flip-flop is proposed and analysed under the Cadence Virtuoso environment (Spectre). Also, the passive components are the main construction units of the electronic circuits and without them, the circuits would become unstable or does not function well. But, these components are bulky in nature and difficult to fabricate on a chip. These facts stress the need for a low area or nano-device known as "Memristor" which can be replaced by the conventional passive components. A 4-bit memristive DAC (Digital to Analog Converter) is constructed using memristors and compared with the conventional 4-bit R-2R DAC.

Keywords: Memristors, non-volatile memory, low power design.

I. INTRODUCTION

The comprehension and first theory of memory-resistor device was proposed by Widrow in 1960 which is now known as "Memristor". It is a passive two-port element with varying resistance which is known as "Memristance" [1].

After a long research and the consequences of his preliminary exceptional work in non-linear circuit theory during 1960s, Prof. L.O. Chua made a remarkable observation that headed to the discovery of the memristor as a Mathematical unit in 1971 [2].

The Memory-resistor (memristor) is a two-terminal device in electronics field, defined by the Ohm's law which is state dependent, i.e., its resistance of a memristor depends on the set of internal state-variables. The encouraging properties of memristive circuit rationalize the modern tremendous progress of the associated research efforts which led to numerous encroachments in the concept and prospective applications of memristors including, among others, computing.

II. MEMRISTOR BIASING

As mentioned before, memristor is a two-terminal passive device which has the ability to remember the charge flowing through the device. The memristor symbol is given in Fig.1(a). The properties of the memristor were characterized by Leon Chua in 1971. The researchers from the HP (Hewlett-Packard) Labs to associate Chua's theory with a fabricated device for the first time [1]. The fabricated device consists of the two layers or deposits of Titanium-di-oxide (TiO_2) with the doped and un doped regions sandwiched between the two electrodes of platinum material and shown in Fig.1.(b), where w is the doped region and D is the full channel length (doped and un-doped regions) of the memristor.

Figure 1. (a). Memristor symbol. (b). Doped and undoped regions.

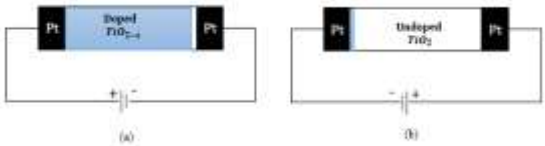


Figure 2. (a). Forward biasing. (b). Reverse biasing.

The doped region consists of oxygen vacancies (TiO_{2-x}). A memristor can be biased by applying appropriate voltages across the device and the resistance (memristance) can be varied accordingly to R_{OFF} which denotes high resistance and R_{ON} which denotes low resistance. To forward bias the memristor, a higher polarity is applied to the doped region and a lower polarity is applied to the un-doped region which enlarges the doped region and decreases the resistance of the device and the memristance will be equal to R_{ON}. To reverse bias the memristor, a higher polarity is applied to the un-doped region and a lower polarity is applied to the doped region which enlarges the un-doped region and the memristance will be equal to R_{OFF} and Fig.2 shows the biasing of a memristor.

III. MODELLING OF THE MEMRISTORS

There are several models of memristors which are defined for the requirements of the applications such as Linear ion drift model, Non-linear ion drift model, Simmons tunnel barrier model, TEAM (ThrEshold Adaptive Memristive model) and VTEAM (Voltage ThrEshold Adaptive Model) [6]. In this paper, Linear ion drift model is considered in order to create

resistance in the circuit using memristor [7] and the manual to use different models is given by [8] and [13]. The modelling of memristor can done using SPICE and Verilog-A language with the aid of [4] and [5].

A. *Linear ion-drift model*

In linear ion drift model, there are two resistors serially connected representing the highly doped area (low resistance) and the low concentration of dopants region which represents the oxide region (high resistance) [9]. In other words, doped region indicates high conductance and un-doped region represents low conductance. In this model, few assumptions are made to give linear ion drift in a uniform field, Ohmic conductance and equal ion mobility.

B. *VTEAM model*

VTEAM stands for Voltage ThrEshold Adaptive Model. This is the global model for the memristors and threshold voltage plays an important role. The crucial part of the VTEAM model is based on the derivative of the internal state variable which fits into any style of the memristive device [11]. In contrast with other memristive models, the relationship of current and voltage is not defined and can be liberally chosen from any current-voltage expressions. This model characterizes the equivalent physical behavior, but with simpler Mathematical expressions given in [12].

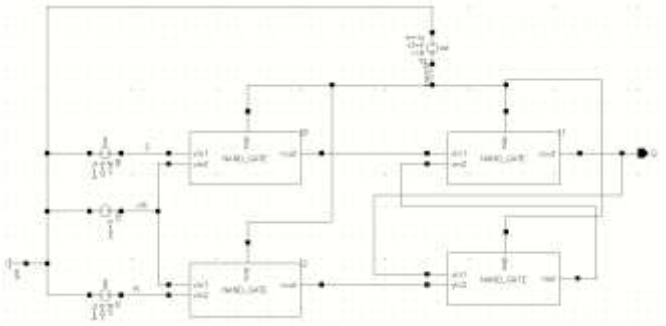


Figure 3. Volatile SR flip-flop

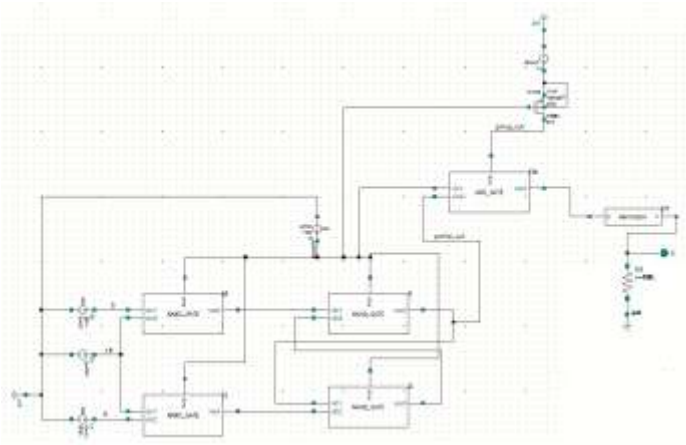


Figure 4. Non-volatile SR flip-flop

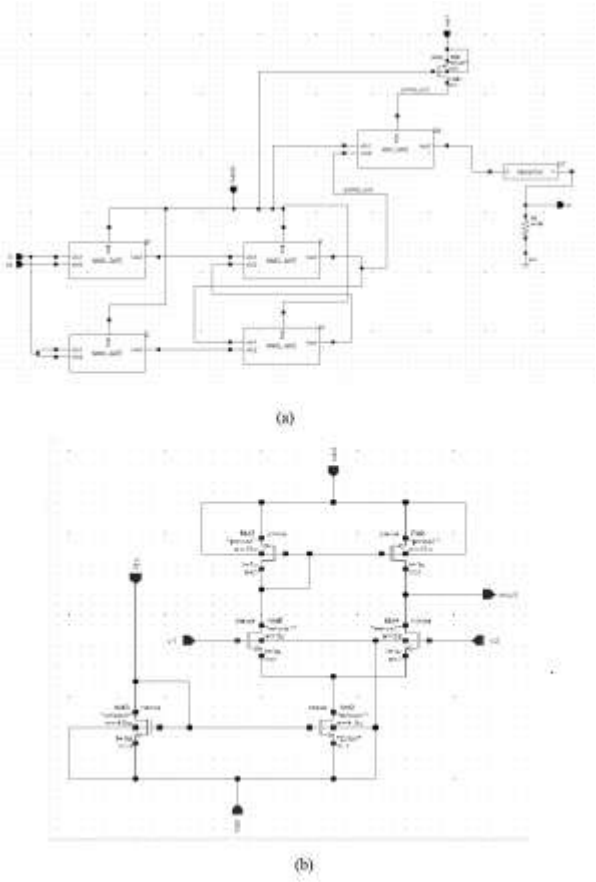


Figure 5. Schematic diagram of (a). D flip-flop for DAC test circuit. (b). OP-AMP.

IV. PROPOSED MEMRISTIVE CIRCUITS

A. *Non-volatile SR flip-flop*

The SR (Set-Reset) flip-flop is one among the simplest sequential circuits which stores 1-bit memory. The schematic diagram of a conventional (volatile) SR flip-flop is given in Fig.3. Here, the data is lost when the power supply is turned off.

To overcome the problem of volatility, a non-volatile flip-flop is constructed where the data will be retained even after the power supply is turned off. This can be done by using a memristor which has the capability to remember the data. The schematic diagram of non-volatile SR flip-flop is given in Fig.4. The non-volatile SR flip-flop was analyzed in [13] which would be difficult to analyze is in higher technologies like 90nm or 45nm since the logic of pass transistors does not hold good in the recent technologies. Due to this reason, SR flip-flop is constructed using NAND gates [15].

The truth-tables of the volatile SR flip-flop and non-volatile SR flip-flop using memristor are given by Table 1 and Table 2 respectively, where PS is the power supply of the circuit, Q^n and Q^{n+1} are the current state and the next state respectively.

Fig.3 functions as a basic SR flip-flop as shown in Table 1. In Fig.4, the input to the PMOS MOSFET lies between the negative and positive threshold voltages of the memristor.

When the main power supply PS goes low, the PMOS is turned on which gives out to the memristor. Since the input to the memristor lies between the threshold voltages, there will be no change in the memristance and hence the previous data is retained which can be seen at the output of the memristor irrespective of the input S and R. When the power supply is ON and if S is 1(0) and R is 0(1), the input to the AND gate from the NAND gate will be 1(0) and hence the output of AND gate will be 1(0) which is fed to the memristor thereby decreasing(increasing) the memristance and hence the memristor acts as a conductor(conductor) giving out Q as 1(0). If both S and R are 0, then the input to the AND gate from NAND remains unchanged (previous state) and hence the memristance remains unchanged and Q will be in the previous state. If both S and R are 1, the outputs of the right most NAND gates are not defined and hence there will be same effect on memristor, but here for simplification, the output is considered to be 1 when both S and R are 1.

Table 1. Truth-table of volatile SR flip-flop

PS	S	R	Q^n	Q^{n+1}	State
1	0	0	0	0	Hold state
			1	1	
		1	0	0	Reset to logic 0
			1		
	1	0	0	1	Set to logic 1
			1		
		1	0	X	Undefined
			1		
0	X	X	X	0	Reset to logic 0

Table 2. Truth-table of non-volatile SR flip-flop

PS	S	R	Q^n	Q^{n+1}	State
1	0	0	0	0	Hold state
			1	1	
		1	0	0	Reset to logic 0
			1		
	1	0	0	1	Set to logic 1
			1		
		1	0	X	Undefined
			1		
0	X	X	X	Q^n	Hold state

B. Digital-to-Analog Convereter (DAC)

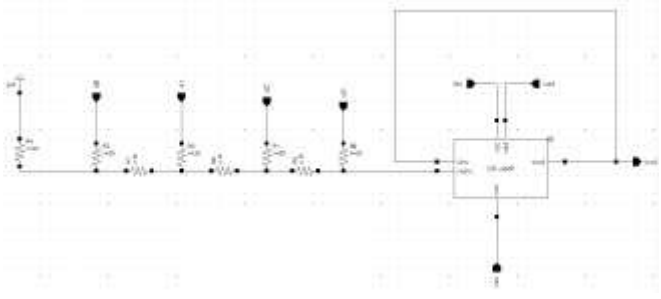
In this DAC, 4-bit R-2R resistor ladder is considered which is an electrical circuit constructed out of repeating resistive components. The 4-bit R-2R network straight way transforms parallel digital signal (symbols or bits) into an analog signal. The digital data adds its weighted impact to the analog signal at the output. This resistive network plays a unique role and consists of properties like the components are scalable easily for any required number of bits, the circuit has only two quantities of resistances which makes the calculations easy and the total impedance at the output is the resistive value chosen (R) irrespective of number of bits considered which makes the signal processing easier further. The typical 4-bit R-2R DAC schematic and its test circuit is given in Fig.6, which uses OP-AMP (Operational Amplifier) circuit where the OP-AM is designed using MOSFET.

In the circuit shown in Fig.5, M1, M2, M7 are the PMOS MOSFETs and M3, M4, M5 M6 are the NMOS MOSFETs where V_{dd} is the power supply, V_{inv} and $V_{non\text{-}inv}$ are the inverted and non-inverted inputs, V_{bias} is the biasing input. The circuit shown in Fig.6.(a) consists of 4-bit R-2R network with OP-AMP which results into an efficient 4-bit R-2R DAC circuit. Though the 4-bit R-2R DAC gives out accurate conversion with good performance, unfortunately the whole circuit cannot be fabricated on a single chip as the resistors are bulky in nature and it also consumes more power. Hence, there comes the need of memristors which is a low power device and can also be easily programmed and fabricated when compared to the conventional 4-bit R-2R DAC. The DAC using 4-bit memristive ladder schematic and its test circuit is given in Fig.7. The OP-AMP schematic for this is same as in Fig.5.

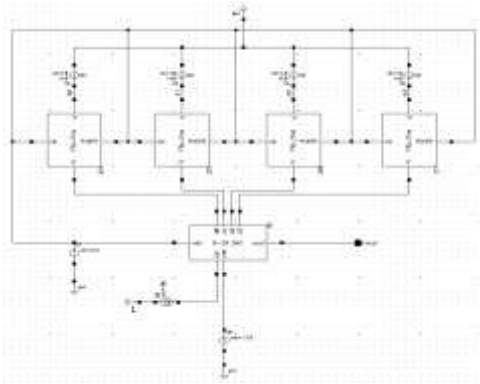
V. SIMULATION RESULTS

A. Simulation results of SR flip-flop

In Fig.5, the memristor is modelled with R_{ON} =1KΩ, R_{OFF} =1MΩ, S, R and PS (power supply) are given as the voltage pulses and Q is the output in both Fig.3 and Fig.4. The transient analysis of the volatile SR flip-flop and nonvolatile SR flip-flop (using memristors) are shown in Fig.8 and Fig.9 respectively.

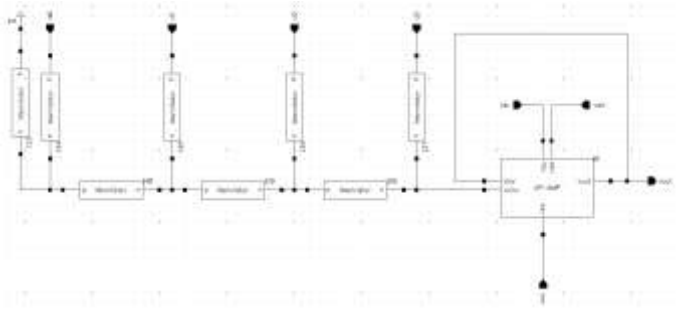


(a)

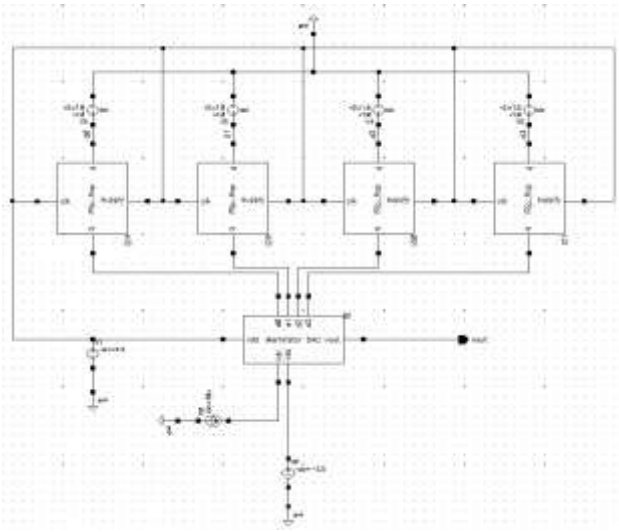


(b)

Figure 6. 4-bit R-2R ladder DAC (a). Schematic diagram. (b). Test circuit.



(a)



(b)

Figure 7. 4-bit Memristive ladder DAC (a). Schematic diagram. (b). Test circuit.

B. Simulation results of DAC

The transient analysis of 4-bit R-2R ladder DAC and 4-bit memristive ladder DAC are proven to be same and it is shown in Fig.10 and their power analysis is shown in Fig.11. It is observed that the transient analysis of 4-bit memristive ladder DAC exactly match with that of conventional 4-bit R-2R DAC. It is also observed that the total power of 4-bit R-2R ladder DAC is in milliwatts and that of the memristive ladder DAC is in micro-watts which indicates that the power is reduced when memristors are used. The comparison between the 4-bit R-2R ladder DAC and memristive ladder DAC is shown in Table 3.

VI. CONCLUSION

A low power programmable 4-bit memristive ladder DAC is constructed and the functionality of the memristive ladder DAC is proven to be same as the conventional 4-bit R-2R DAC and the non-volatile SR flip-flop using memristors is constructed and compared with the conventional volatile SR flip-flop. Apart from these characteristics, memristors can be fabricated on a chip thereby reducing a lot of area of the overall system.

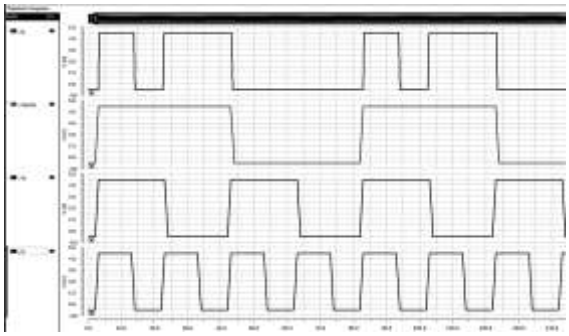


Figure 8. Transient analysis of the volatile SR flip-flop.

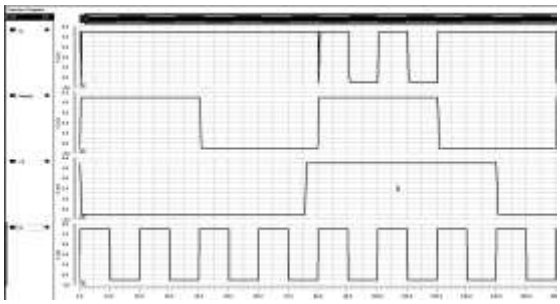


Figure 9. Transient analysis of the non-volatile SR flip-flop.

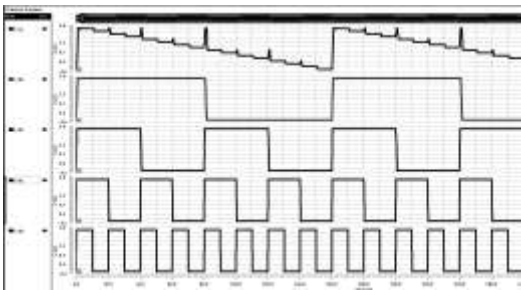


Figure10. Transient analysis of the 4-bit R-2R ladder DAC and memristive ladder DAC.

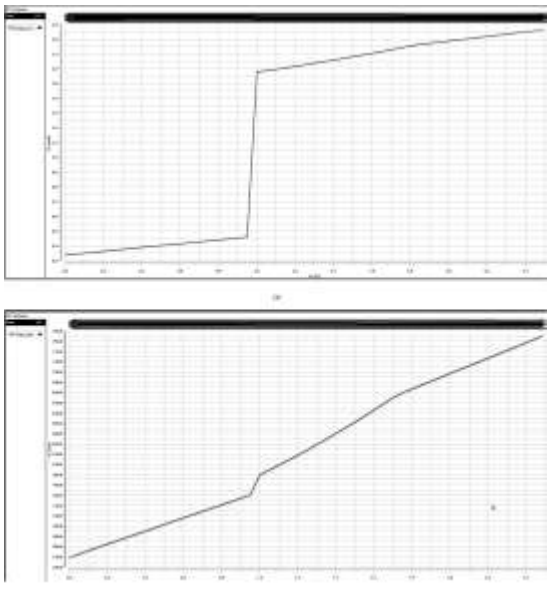


Figure 11. Power analysis of (a). 4-bit R-2R ladder DAC. (b). 4-bit memristive ladder DAC.

Table 3. Comparison between the 4-bit R-2R ladder DAC and 4-bit memristive ladder DAC

Properties / Type	Total power of the circuit	On-chip fabrication
4-bit R-2R DAC	At lower frequencies: 342uW At higher frequencies: 1.9mW	Not capable
4-bit Memristive DAC	At lower frequencies: 340uW At higher frequencies: 765uW	Capable

ACKNOWLEDGMENT

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