International Journal of Modern Electronics and Communication Engineering (IJMECE) ISSN: 2321-2152
Volume No.-7, Issue No.-3, May, 2019

10 Bit Addressable Multi Master I2C Protocol

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Abstract: This paper presents the working of a 10 bit addressed slave supportable I2C protocol for multi master multi slave operation. Arbitration technique is used to determine which master to hold the bus for communication on I2C network .The I2C protocol has been implemented by satisfying DO-254 standards and rules such that the implemented I2C protocol have higher reliability and reusability .To implement the I2C protocol mentor graphics HDL designer, Questasim and Precision RTL tools were used in project implementation flow

Keywords: DO-254, I2C, Arbitration

I. INTRODUCTION

From the past decade the number of features that can be incorporated in the in a circuit are rapidly increasing and the efficiency of these modules (features) can be increased by using an efficient communication protocol in circuit .There are two types of communication protocols they are parallel and serial communication protocol, the serial communication protocol are comparatively efficient and consume less area compare to parallel communication protocol .In serial communication protocols the I2C is one of the serial wired communication protocol which is the efficient and most robust communication protocol which support multi master multi slave communication.

The I2C protocol consume less area than others since it uses only two wire i.e. SDA(serial data) line and (SCL) serial clock line to communicate with masters and slaves The I2C serial communication reduces the cost of connection and the number of IC pins. I2C protocol can be used in different control architectures such as Power Management Bus, System Management Bus, Display Data Channel and Advanced Telecom Computing Architecture, analog to digital converter (ADC) etc.

In this paper represents the Verilog implementation of multi master multi slave I2C protocol which supports the communication between masters and 10 bit addressed slaves. The design of the protocol was done under the DO-254 design assurance standards, such that it can be used in avionic controllers and military application.

The outline of this paper is as follows. In section II the 10 bit addressing and arbitration mechanism in I2C protocol and the implementation of multi master multi slave I2C is presented which incorporates Arbitration and 10 bit addressing mechanism. Section III shows the results acquired during the simulation .finally section IV presents the conclusion, followed by reference section

II. METHODOLOGY

A. ARBITRATION AND 10 BIT ADDRESSING MECHANISM IN I2C

I2C communication protocol uses are only two line (SDA and SCL) to communicate between master and slave so when it comes to multi master consideration it is mandatory to know which master should have access to SDA(serial data) line .To know this Arbitration mechanism is used

When more than one master are trying to access the bus simultaneously, arbitration procedure will decide which master to continue the communication with slave .arbitration is occurred only during start condition and data transfer

In I2C protocol bidirectional SDA and SCL line are connected to VDD using the pull up resistor therefore the master which pulls SDA line to low (zero)will win the arbitration and other masters will lose arbitration as shown in the figure given below

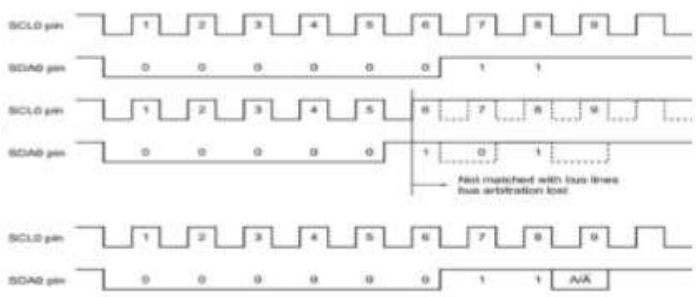

Figure1. Arbitration lost during data transfer

10 bit addressing: 10 bit addressing will increase the number of possible addresses. Devices of 7 bit and 10 bit address can be connected using same i2c serial data line and serial clock line.10 bit address can be accessed by the first two bytes after start condition. The first five bits of first byte will be "11110" which will 10 bit addressing identifier .the first two bytes format is as shown below

FIGURE2.10 BIT ADDRESSING FROMAT

When the master transmits first byte of address to SDA line the slaves receives the address and compares with its address if the address is matched the slave sends ACK bit as 0 and continue to receive the data where other slave will go to ideal state, when it comes to 10-bit address transfer after first byte address transfer the 7-bit slave will go ideal state and according to next byte the 10-bit addressed slave compares to its address and if it address matches then respective slave will send the ACK bit as "0" else it will sends negative ACK as"1"

B. IMPLEMENTATION OF I2C MASTER

The below figure represent a detailed view of I2C master. The master contains a wishbone interface which is used to interface the micro-control signal to Bit-Byte controller module. Bit-Byte controller module is used to convert parallel data sent by micro controller to serial data and is sent on SDA line accordinglyclock pulse is generated on SCL line

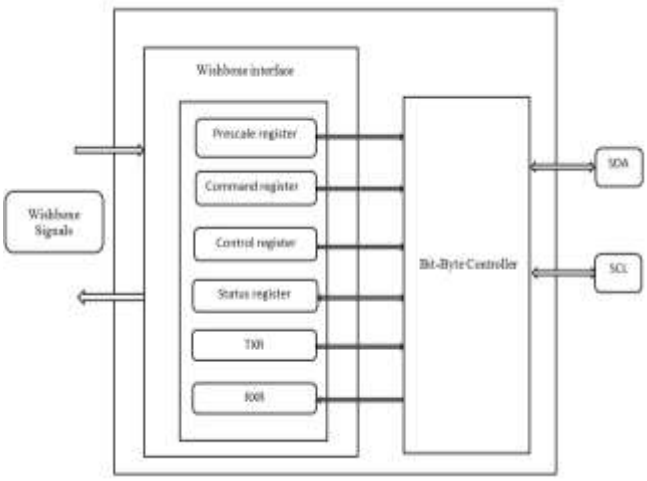

FIGURE3.MASTER ARCHITECTURE

The wishbone interface has six internal registers which used for I2C communication purpose. Based on the command register and control register the serial transfer of data takes place which is as shown in below figure below.

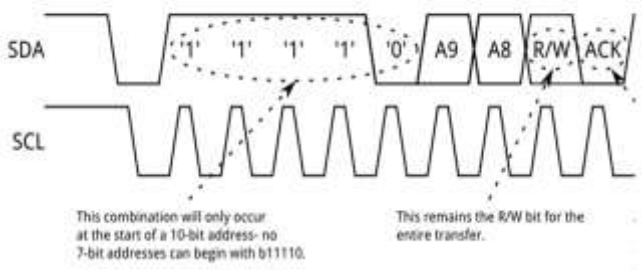

FIGURE4.**10 bit address identifier**

According to start and stop condition the data transfer occurs in I2C, a transition of high to low on the SDA line while SCL is high defines a start condition. After start condition if the master wants to communicate with 10 bit addressed slave then the first 5 bits should be in combination as shown in the figure given above, the 6th and 7th bits will be address bit 9 and 8 of slave and then followed by a read/write bit. After 8 bit transfer there will be an acknowledgment sent by the slave as a response. The next byte will be the remaining 8 bit address of slave as shown below waveform. The data transfer will be same as in the 7 bit addressed slave as in the reference [4]

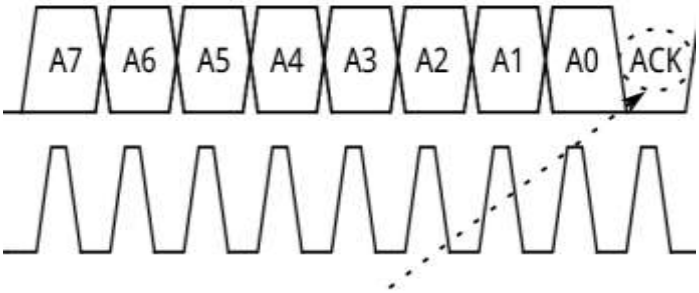

FIGURE5.**Ack after 8 bits**

III. EXPERIMENTAL RESULTS

For the implementation of this paper mentor graphics HDL designer, Questa Sim and precision RTL tools were used. HDL designer as design checker unit [8] which have designer policies such as DO-254, Altera policy, vertices policy etc. which is actually used for checking the standards of the design according to respective policy. In this paper the implementation of design was done under the standards of DO-254 policy and result of the design checker was 98% design quality with no errors as shown in figure 6

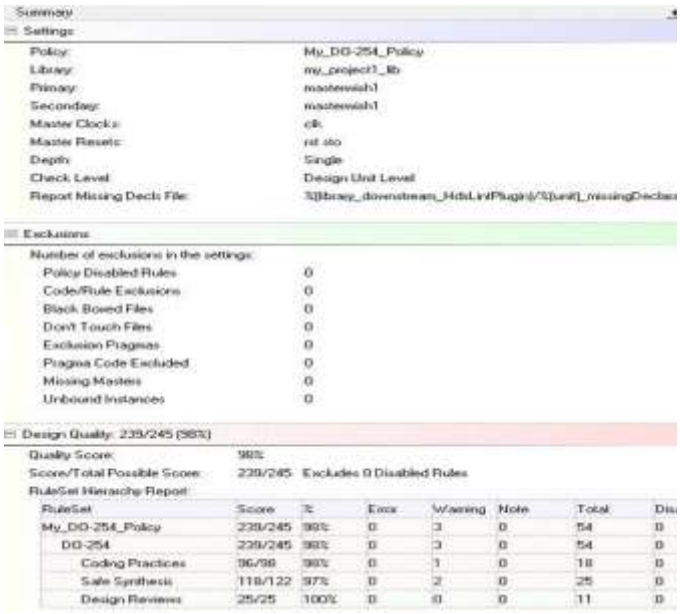

FIGURE6.**Design quality under DO-254 policy**

QuestaSim is the mentor graphic simulator [9] and it is also used for verification and trace out of the entire design as shown in the figure below

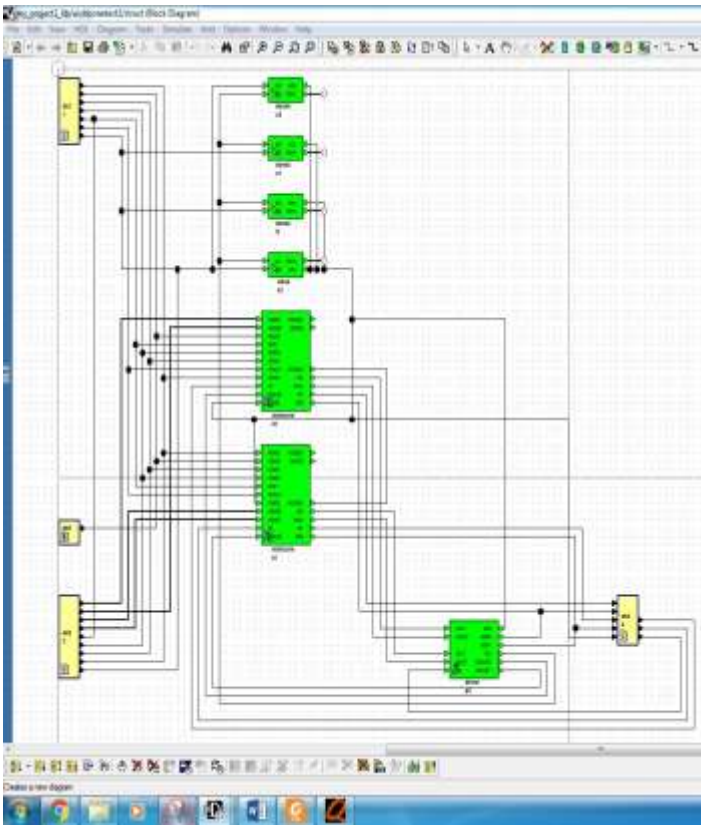

FIGURE7.**Schematic trace out of Questasim**

The below figure shows the i2c master and 10 bit addressed slave communication

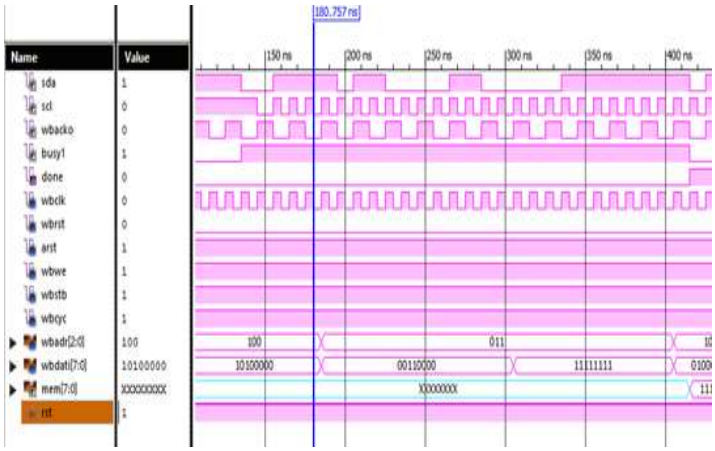

FIGURE8.**Master communicate with 10 bit addressed slave**

Figure9 shows the arbitration lost during data transfer. Here Master1 losses its arbitration since the master 2 will first pull the SDA line to "0"

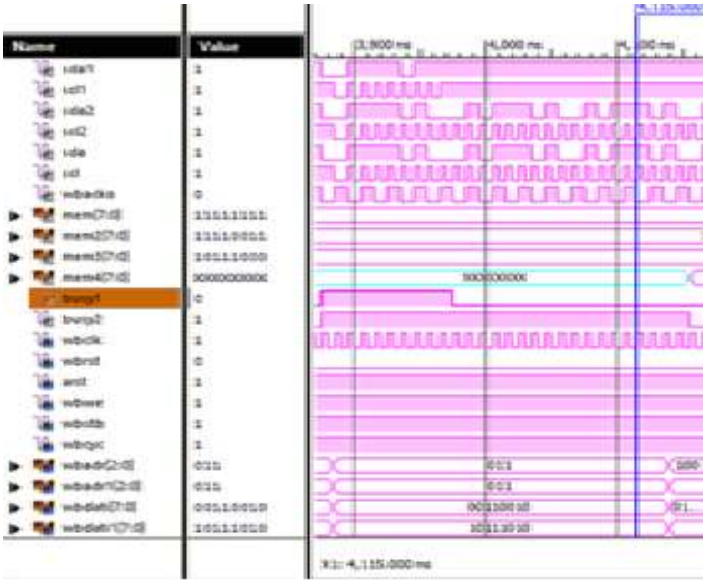

FIGURE9. **Master1 Arbitration lost during data transfer**

IV. CONCLUSION

The 10 bit addressed slave supportable multi master I2C was implemented using the arbitration mechanism the implemented design satisfies the DO-254 standards. Since the implemented protocol satisfies DO-254 standards and rules it is more reliable and reusable and it can be used in real time applications, the total power required by the implemented design is comparatively reduced than the previous paper [4].

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