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A Quantitative Report On: Input-Output Standards Based ROM Design for IoT application

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Abstract: Recently, the demand of portable devices with low power consumption and high performance are increasing in today life. The low power utilization for every activity is a standout amongst the most essential prerequisites for easily movable gadgets.
In this paper , Read only memory (ROM) are design for core i7 frequencies 1.0,2.9,3.3,4.0(GHz) range with the help of different I/O standard family i.e LVDCI, SSTL and HSTL and compare the power dissipation with the above frequency. It has been seen that at maximum frequency LVCMOS have 14% and 41.2% less power dissipation with respect to HSTL and SSTL input output (IO) standards at 65nm technology.

Keywords: I/O standards, LVDCI, HSTL, SSTL, ROM, FPGA.

I. INTRODUCTION

Now a day, high performance integrated circuits are being implemented in deep sub-micron technology. Read only memory (ROM) is one of them. Usually in the ROM data is written at the time of fabrication of memory. The data is permanently fix and cannot performer re-write operation. In the ROM the data is not depend on supply voltage. It mean if the supply voltage is off the data will not be lost. It works in washing machine, BIOS in computer system, Microwave etc.ROM retains its contents even when the power is turned off.

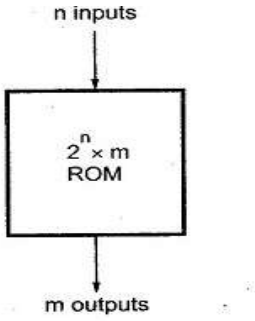

Figure 1:Block diagram of ROM

ROM has n input and m output. In general, a 2^n x m defines that decoder and OR gates for input and output for the data.Decoder size is defines as n x 2^m and m numbers of OR gates is required. Each OR gate has 2^n inputs, which are connected to each of the outputs of the decoder.

1. FPGA:

Field Programmable Gate Array or FPGA is a device that is widely used in the digital electronic. The advantage of the FPGA is that the chip is completely programmable and can be re-programmed.

DIFFERENT TYPE I/O STANDARD:

1. Low Voltage Digital Control Impendence (LVDCI)
2. Stub Series Terminated Logic(SSTL)
3. High Speed Transceiver Logic (HSTL)
4. Low Voltage Transistor-Transistor Logic (LVTTL)
5. Mobile Double data rate(Mobile-DDR)

1. **Low Voltage Digital Control Impendence (LVDCI):**It is a type of *I/O* standard. It has also divided into five categorize.

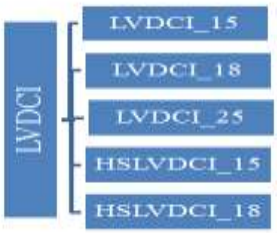

Figure 2: Family of LVDCI

Here LV stands for Low voltage and HS stands for High voltage and DCI stands for Digitally Control Impedance. In this paper this technique is used for calculating power dissipation. There are two sources of power dissipation:

i. Dynamic power dissipation
ii . Static power dissipation

2. **Stub Series Terminated Logic (SSTL):** It is also a type of I/O standard. It has classified into five categories:

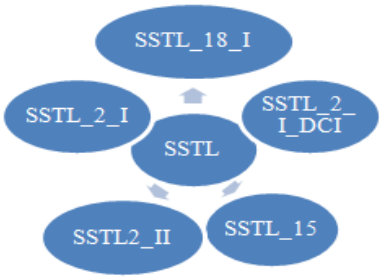

Figure 3: Family of SSTL

3. **High Speed Transceiver Logic(HSTL):**It is a type of I/O standard. It is also divided into five categorize:

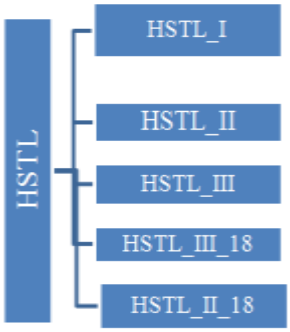

Figure 4: Family of HSTL

4. **Low Voltage Transistor-Transistor Logic(LVTTL):**It is a type of I/O standard. it is also divided into three categorize:

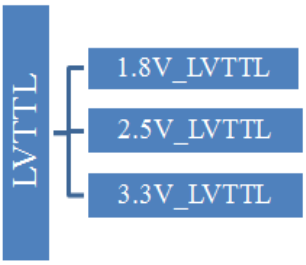

Figure 5: Family of LVTTL

5. **Mobile Double data rate(Mobile-DDR):**It is a type of I/O standard. It is also divided into six categorize:

Figure 6: Family of M-DDR

II. LITERTURE REVIEW

In this section we discuss about some paper which have use some different I/O standard for energy efficient ROM design on FPGA. In first paper when LVDCI I/O standard are used at Virtex-5 FPGA using Verilog hardware description language and Xilinx ISE simulator for designing ROM on FPGA.[1] we see that there is reduction in total power, clock power and signal power at different frequency. LVDCI has also different-different I/O standard. In different I/O standard there is no reduction in clock power and signal power but total power is reduced.

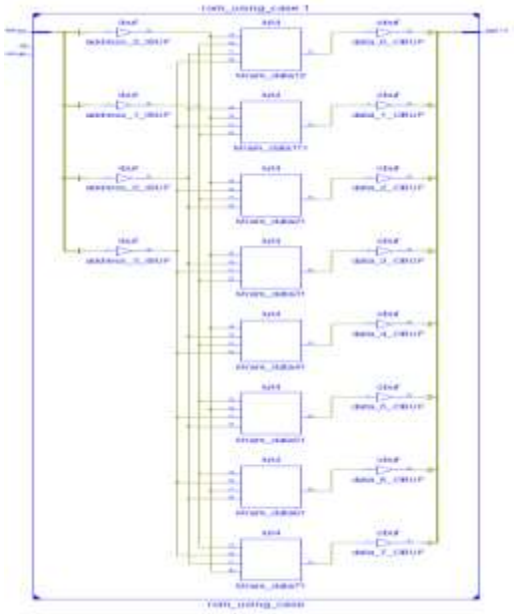

Figure 7: RTL Schematic of ROM

In second paper when HSTL I/O standard are used at Virtex-5 FPGA using Verilog hardware description language and Xilinx ISE simulator for ROM design on FPGA [5].we see that there is reduction in total power clock power and signal power when frequency is scaling down, but HSTL_III_DCI has no reduction in clock power and signal power as comparison of different type of HSTL I/O standard.

In third paper when SSTL I/O standard are used at Virtex-6 FPGA using Verilog hardware description language and Xilinx ISE simulator for ROM design on FPGA.[6] we see that there is reduction in total power as well as clock power and signal power when scaling in frequency, but there is no change in clock power and signal power at SSTL2_II_DCI at 3.3 GHZ frequency as comparison to other SSTL I/O standard. In fourth paper LVTTL & M-DDR both I/O standard are use at Artix-7 FPGA using Verilog hardware description language and Xilinx ISE simulator for Designing of Power Efficient ROM[7,3].we see that there is reduction in there is reduction in clock power signal power and total power when the frequency is scale down. when we compare LVTTL & M-DDR I/O standard at

different frequency we see that M-DDR consume less power than LVTTL.

III. COMPARISON

In this section we compare the different I/O standard with given different frequency for clock power ,signal power,i/o power and total power dissipation

- **At Frequency 1 GHz**

Table 1: Dissipation of Power with different LVDCI [1]

Power→ LVDCI↓	Clock	Signal	IOs	Total
LVDC_15	0.010	0.001	0.039	0.428
LVDCI_18	0.010	0.001	0.061	0.450
LVDCI_25	0.010	0.001	0.126	0.517
HSLVDCI_15	0.010	0.001	0.055	0.443
HSLVDCI_18	0.010	0.001	0.087	0.476

Table 2: Dissipation of power with Different HSTL [5]

Power→ HSTL↓	Clock	Signal	IO	Total
HSTL_I	0.010	0.000	0.156	0.545
HSTL_II	0.010	0.000	0.256	0.647
HSTL_III	0.010	0.000	0.209	0.599
HSTL_III_18	0.010	0.000	0.209	0.600
HSTL_III_DCI	0.010	0.000	0.282	0.674
HSTL_II_18	0.010	0.000	0.256	0.648

Table3: Dissipation of Power with Different SSTL [6]

Power→ SSTL↓	Clock	Signal	IO	Total
SSTL2_I	.013	.001	0.471	1.208
SST18_I	.013	.001	0.413	1.148
SSTL2_I_DCI	.013	.002	1.035	1.786
SSTL2_II	.013	.001	.551	1.290
SSTL15	.013	.001	.393	1.127
SSTL2_II_DCI	.013	.002	3.014	3.816

The above table so the dissipation of different power at different I/O standard family at same frequency 1GHZ.From above table we find out that:

- ❖Clock power dissipation of HSTL and LVDCI family are same but SSTL family are low.
- ❖Signal power dissipation of LVDCI and SSTL family are almost same but HSTL family has 0.00 signal power
- ❖IOs power dissipation of SSTL are more than HSTL and HSTL power dissipation is more than LVDCI family.
  - LVDCI<HSTL<SSTL
- ❖Total power dissipation of SSTL are more than HSTL and HSTL power dissipation is more than LVDCI family.
  - LVDCI<HSTL<SSTL

- **At Frequency 2.9 GHz**

Table 4: Dissipation of Power with Different LVDCI [1]

Power→ LVDCI↓	Clock	Signal	IOs	Total
LVDCI_15	0.051	0.002	0.060	0.491
LVDCI_18	0.051	0.002	0.087	0.519
LVDCI_25	0.051	0.002	0.165	0.600
HSLVDCI_15	0.051	0.002	0.074	0.506
HSLVDCI_18	0.051	0.002	0.112	0.545

Table 5: Power Dissipation with Different HSTL [5]

Power→ HSTL↓	Clock	Signal	IO	Total
HSTL_I	0.051	0.001	0.166	0.599
HSTL_II	0.051	0.001	0.264	0.698
HSTL_111	0.051	0.001	0.224	0.657
HSTL_III_18	0.051	0.001	0.227	0.661
HSTL_III_DCI	0.051	0.001	0.298	0.732
HSTL_II_18	0.051	0.001	0.266	0.700

Table 6: Power Dissipation with Different SSTL [6]

Power→ SSTL↓	Clock	Signal	IO	Total
SSTL2_I	0.037	0.003	0.581	1.348
SST18_I	0.037	0.003	0.493	1.257
SSTL2_I_DCI	0.037	0.005	1.127	1.909
SSTL2_II	0.037	0.003	0.736	1.506
SSTL15	0.037	0.003	0.497	1.260
SSTL2_II_DCI	0.037	0.005	3.093	3.926

The above table so the dissipation of different power at different I/O standard family at same frequency 2.9 GHZ. From above table we find out that:

- ❖Clock power dissipation of HSTL and LVDCI family are same but SSTL family are low.
- ❖Signal power dissipation of LVDCI and SSTL family are almost same but HSTL family has 0.00 signal power
- ❖IOs power dissipation of SSTL are more than HSTL and HSTL power dissipation is more than LVDCI family.
  - LVDCI<HSTL<SSTL

❖Total power dissipation of SSTL are more than HSTL and HSTL power dissipation is more than LVDCI family.

- LVDCI<HSTL<SSTL

- **At Frequency 3.3 GHz**

Table7: Power Dissipation with different LVDCI[1]

Power→ LVDCI↓	Clock	Signal	IOs	Total
LVDCI_15	0.072	0.002	0.064	0.518
LVDCI_18	0.072	0.002	0.092	0.547
LVDCI_25	0.072	0.002	0.173	0.630
HSLVDCI_15	0.072	0.002	0.079	0.533
HSLVDCI_18	0.072	0.002	0.118	0.573

Table 8: Reduction of Power with Different HSTL [5]

Power→ HSTL↓	Clock	Signal	IO	Total
HSTL_I	0.072	0.001	0.169	0.624
HSTL_II	0.072	0.001	0.265	0.722
HSTL_111	0.072	0.001	0.227	0.683
HSTL_III_18	0.072	0.001	0.230	0.687
HSTL_III_DCI	0.072	0.001	0.301	0.757
HSTL_II_18	0.072	0.001	0.268	0.724

Table 9: Reduction of Power with Different SSTL[6]

Power→ SSTL↓	Clock	Signal	IO	Total
SSTL2_I	0.042	0.004	0.616	1.389
SST18_I	0.042	0.004	0.518	1.288
SSTL2_I_DCI	0.042	0.006	1.156	1.945
SSTL2_II	0.042	0.004	0.732	1.573
SSTL15	0.042	0.004	0.529	1.299
SSTL2_II_DCI	0.042	0.006	3.118	3.9570

The above table so the dissipation of different power at different I/O standard family at same frequency 3.3GHZ.From above table we find out that:

- ❖ Clock power dissipation of HSTL and LVDCI family are same but SSTL family are low.
- ❖ Signal power dissipation of LVDCI and SSTL family are almost same but HSTL family has 0.00 signal power
- ❖ IOs power dissipation of SSTL is more than HSTL and HSTL power dissipation is more than LVDCI family.

  LVDCI<HSTL<SSTL
- ❖ Total power dissipation of SSTL is more than HSTL and HSTL power dissipation is more than LVDCI family.

  LVDCI<HSTL<SSTL

- **At Frequency 4.0 GHz**

Table 16: Reduction of Power with Different LVDCI [1]

Power→ LVDCI↓	Clock	Signal	IOs	Total
LVDCI_15	0.128	0.002	0.072	0.583
LVDCI_18	0.128	0.002	0.102	0.614
LVDCI_25	0.128	0.002	0.188	0.702
HSLVDCI_15	0.128	0.002	0.086	0.597
HSLVDCI_18	0.128	0.002	0.128	0.640

Table 17: Reduction of Power with Different HSTL [5]

Power→ HSTL↓	Clock	Signal	IO	Total
HSTL_I	0.128	0.002	0.173	0.684
HSTL_II	0.128	0.002	0.268	0.781
HSTL_111	0.128	0.002	0.233	0.745
HSTL_III_18	0.128	0.002	0.237	0.750
HSTL_III_DCI	0.128	0.001	0.306	0.819
HSTL_II_18	0.128	0.002	0.271	0.785

Table 18: Reduction of Power with Different SSTL[6]

Power→ SSTL↓	Clock	Signal	IO	Total
SSTL2_I	0.051	0.004	0.681	1.466
SST18_I	0.051	0.004	0.565	0.726
SSTL2_I_DCI	0.051	0.007	1.209	2.010
SSTL2_II	0.051	0.004	0.907	1.698
SSTL15	0.051	0.004	0.590	1.372
SSTL2_II_DCI	0.051	0.007	3.164	4.014

The above table so the dissipation of different power at different I/O standard family at same frequency 4.0GHZ.From above table we find out that:

- ❖ Clock power dissipation of HSTL and LVDCI family are same but SSTL family are low .
- ❖ Signal power dissipation of LVDCI and SSTL family are almost same but HSTL family has 0.00 signal power
- ❖ IOs power dissipation of SSTL is more than HSTL and HSTL power dissipation is more than LVDCI family.

  LVDCI<HSTL<SSTL
- ❖ Total power dissipation of SSTL are more than HSTL and HSTL power dissipation is more than LVDCI family.

  LVDCI<HSTL<SSTL

IV. CONCLUSION

As discussed from the above table we conclude that the clock power of SSTL family is low as comparison to LVDCI and HSTL as the frequency scale down. HSTL family has low signal power as frequency is scale down; LVDCI has I/O power and total power as comparison to other family at different frequency.

REFERENCES

[1] Rishita Saini, Neha Bansal "Low Power High Performance ROM Design on FPGA using LVDCI I/O Standard"IEEE International Conference on Computational Intelligence and Communication Networks 2014,Pages:935-938 DOI: 10.1109/CICN.2014.197

[2] Virtex6FPGASelectIOResourcesUserGuide.http://www.xilinx.com/support/documentation/userguides/ug361.pdf

[3] Jue Wang, Xiangyu D, Yuan Xie " Enabling High-Performance LPDDRx-Compatible MRAM" IEEE/Acm International Symposium On Low Power Electronics And Design(Islped)2014,Pages: 339 344, DOI: 10.1145/2627369.2627610

[4] D. Blaauw, S.Martin, T. Mudge, and K. Flautner. "Leakage current reduction in VLSI systems."Journal of Circuits, Systems, and Computers 11, no. 06 (2002): 621-635.

[5] Meenakshi Bansal, Rishita Saini,"HSTL I/O Standard Based Environment Friendly Energy Efficient ROM Design on FPGA"IEEE 2nd International Conference on Computing for Sustainable Global Development (INDIACom) 2015,Inspec Accession Number: 15110140 Pages: 1818 – 1823 .

[6] Meenakshi Bansal, NehaBansal"SSTL I/O Standard Based Environment Friendly Energy Efficient ROM Design on FPGA ." IEEE 3rd International Symposium on Environmental Friendly Energies and Applications (EFEA) 2014,Pages: 1 – 6 DOI: 10.1109/EFEA.2014.7059947.

[7] Anjan Lumar,Vivek Agrawal "LVTTL I/O Standard Based Environment Friendly Energy Efficient ROM Design on FPGA" .IEEE International Conference on Computational Intelligence and Communication Networks (CICN)2015.Pages:1334- 1337, DOI: 10.1109/CICN.2015.257

[8] lakshay kalra, neha bansal, rishita saini " LVCMOS I/O Standard Based Environment Friendly Low Power Rom Design On Fpga " IEEE 2nd International Conference On Computing For Sustainable Global Development (Indiacom)2015, Pages:1824 – 1829 Inspec Accessionnumber: 15110063.

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