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Design and Simulation of High Performance Three Stage Operational Amplifier at 32 nm

M Nizamuddin
Jamia Millia Islamia
New Delhi , India
E-mail: nizamdelhi25@gmail.com

Abstract: In this paper, CMOS technology based three stage op-amp. is proposed. The DC gain, bandwidth, input resistance, output resistance and unity gain frequency (UCF) of the proposed CMOS based three stage op-amp are studied. The proposed three stage op-amp was designed at 32nm technology using LTSPICE simulator.

Keywords—CMOS, CMOS-FET, DC Gain, UGF.

I. INTRODUCTION

The single stage operational amplifier is a differential pairs that permit the straight pass the small signal currents generated through the input differential pairs across the output impedance. Thus, they limit the gain of their particular topologies that are multiplication of input pair trans-conductance and the output impedance. Although such gain in these circuit could enhanced by the employ of cascade of these circuit, the output fluctuation of such op-amps are else restricted due to adding up of transistor stages. Usually this restriction needs to be assigned as the gain and for voltage fluctuation presented by the cascaded amplifiers are not enough to the desired utilization. While in these case we have alternatives for three stages op-amps it deals along with gain as well as output swing restrictions. However in these configurations usually the first stage generates a large gain and it gives high swing later.

A. Verma et. al. [2] conducted experiment which includes model test of design of two stage CMOS operational amplifier and find out its results according to design parameter. The results of the op-amps shows its drain current, power dissipation, gain of the device, and unity gain frequency and bandwidth of circuit.. L. Selmi et. al. [2] studied DC performance of sub-threshold CMOS logic for ultralow power from the point of view of circuit design. Hence, it gives an useful execution of small signal along with the larger signal models for sub-threshold section operations of MOS transistors. In conventional devices when channel length becomes shorter than depletion width then short channel effect occurs. Short channel includes GIDL, hot electron effect, DIBL, impact ionisation, velocity saturation. A. Amara et. al. [3] performed a layout structure of planar double gate transistor and show how fin hold the source and drain channel three dimensionally on all side and created two gate terminal device.

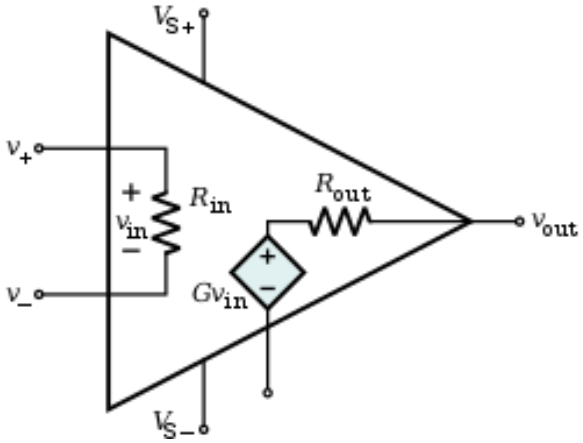

Figure 1 Symbol of Operational Amplifier.

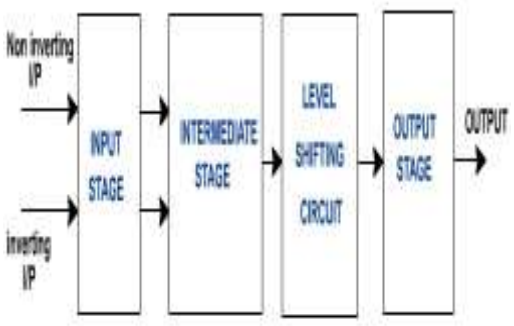

Figure 2. Block diagram of Operational Amplifier.

S.No.	CMOS
1.	M1 = 58
2.	M2 = 58
3.	M3 = 14
4.	M4 = 18
5.	M5 = 26
6.	M6 = 29
7.	M7 = 29
8.	M8 =102
9.	M9 = 05
10.	M10 = 14
11.	M11 = 14

Figure 3. W/L ratio of CMOS transistors, used in proposed structure of CMOS based three stage operational amplifier.

II. PROPOSED CMOS BASED THREE STAGE OP-AMPS.

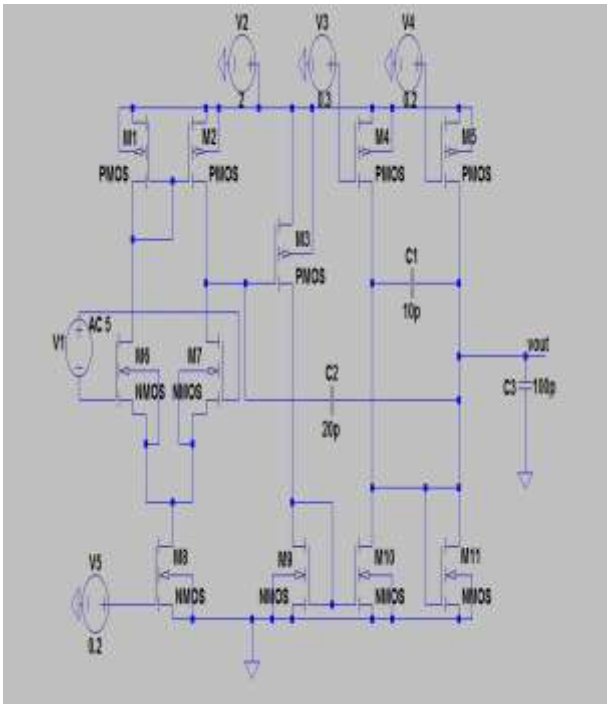

Figure 4. Proposed Schematic of CMOS based three stage op-amp

Figure 4 demonstrates Proposed CMOS based three stage op-amp. This circuit is simulated using LTSPICE at 32nm, with 2V VDD.

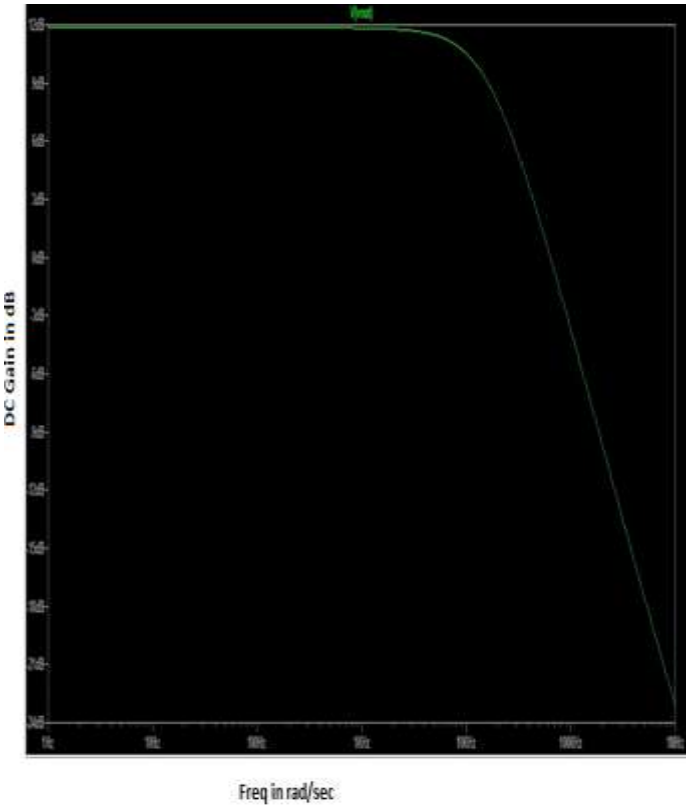

Figure 5. Gain of Proposed Schematic of CMOS based three stage operational amplifier.

The proposed CMOS based op amp designed at 2V provides, DC gain of 11.50 dB, bandwidth of 92.53 KHz, input impedance of 4.48×10^{8} ohm and output impedance of 472 ohm .

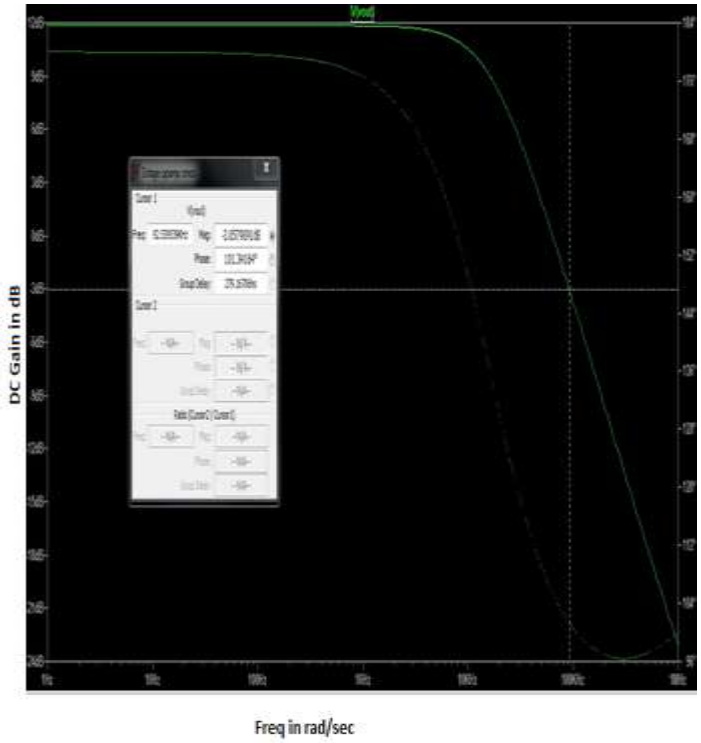

Figure 6. Bandwidth of Proposed Schematic of CMOS based three stage operational amplifier.

Table 1: Simulation study proposed of CMOS based three stage Op-Amp @ 32 nm tech. node at 2V.

S. No.	Parameters	CMOS based three stage Op-Amp
1.	**Gain**	11.50 dB
2.	**Input Resistance**	4.48×10^{8} ohm
3.	**Output Resistance**	472.61 ohm
4.	**Bandwidth**	92.53 KHz
5.	**UGF**	63.36 KHz

III. CONCLUSION

In this paper, three stage operational amplifier structures are designed and simulated at 32 nm technology node. In simulated amplifier the load capacitance was consider as 100 pF and the compensation capacitors C1 and C2 are 20pF and 10pF respectively, so the 32nm technology. AC and transient analysis are performed to calculate and find the different performance measuring parameters of the proposed three stage operation amplifiers.

Result shows that Proposed Schematic of CMOS based three stage operational amplifier is able to deliver more gain, better input and output resistance and high bandwidth as short channel device. The gain, bandwidth, input & output resistance, unity gain frequency of the proposed three stage op-amp are suitable for instrumentation.

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AUTHOR'S BIOGRAPHY

Dr. M. Nizamuddin has completed Ph.D. from JMI, New Delhi, India.He is associated with JMI, New Delhi, India. His field of interest include VLSI, Devices & Nanoelectronic Circuits and Embedded System.