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# Design and Simulation of 4-Bit Parallel Adder using Minimum Number of Transistors

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**Abstract:** Dynamic logic families offer good performance over traditional CMOS logic due to ease of implementation, less propagation delay, and less number of CMOS logic. The drawbacks of dynamic logic families are charge sharing, charge leakage, lack of design automation etc. But these drawbacks can be eliminated using GDI (Gate Diffusion Input) cell. This paper proposes a new design technique of XNOR gate and 4-bit parallel adder using GDI cell which require less number of transistors. The design claims less area, high speed and low power. The simulation results show the novelty of the paper. The simulation is done using DSCH 3.5. A comparative study of the proposed technique has been dealt here with traditional CMOS logic.

**Keywords:** CMOS Logic, Full Adder, GDI Cell, XNOR Gate, DSCH 38.

## I. INTRODUCTION

With rapid development of portable digital applications, the demand for low power dissipation, increasing speed, compact implementation circuits increases. The performances of logic circuit based on CMOS technology have been improved greatly during the last decade. Pass transistor logic is one example of low power design. Dynamic logic circuits are widely used in low power VLSI circuits. One popular advantage of dynamic circuit over static CMOS circuits is their speed. However design using dynamic circuits presents a problem to CAD tools and introduces issues of delay and skew into the circuit design process [1]. The number of transistors which are used to implement different logic gates largely effects the design, speed and power consumption. Different logic families such as complementary MOS (CMOS), pseudo nMOS, transmission gates, dynamic CMOS logic, pass transistor logic etc. are used to design different logic gates to improve the performance. CMOS technology is widely used because of their low power consumption, high speed to power ratio and low cost. But there are significant disadvantages like difficult in implementation. The advantages of pseudo nMOS logic are their high speed and low transistor count but the static power consumption of the pull up transistor of this logic is high as well as output voltage swings and gain of this circuit are not up to the satisfactory limit [2]. Transmission gate CMOS (TG) uses transmission gate logic to realize complex logic functions using reduced number of complementary transistors. It solves the problem of low logic level swing by using pMOS as well as nMOS [1]. TG avoid the problems of reduced noise margin, increase switching resistance and increased static power dissipation caused by increased threshold voltage but it offers lower speed time-skew problems. On the other hand, static CMOS logic circuits using nMOS pulldown and pMOS pullup networks require more number of transistor than dynamic CMOS logic. Static power loss in dynamic CMOS logic is very less and its switching speed is faster than static CMOS logic. But the disadvantages of dynamic CMOS is that it requires more number of transistor than GDI (Gate Diffusion Input) and it needs a clock for the correct working of the circuit. In case of pass transistor logic (PTL), though the transistors count is less, the difference of the voltage between high and low logic levels decreases at each stage and each transistor in series is less saturated at its output than at its input. Another problem of PTL is top-down logic design complexity, which prevents the pass transistors from capturing a major role in real logic LSIs [3]. One of the main reasons for this is that no simple and universal cell library is available for PTL-based design. Many PTL circuit implementations have been proposed in the literature [4] – [9]. From the above discussion, it is clear that the speed, power dissipation and transistor count are the main aspects for the researcher. GDI technique offers high speed, low power consumption and less transistor count. Arkadiy Morgenshtein et. al. proposed in [10], a low power design technique using GDI. GDI approach offers implementation of a wide range of complex logic function using only two transistors. They claim that GDI technique is suitable for design of fast low-power circuits using reduced number of transistors as compared to CMOS and PTL. It improves logic level swing and static power characteristics and allows simple top-down design by using small cell library. R. Uma in [11] proposed a design of 4-bit parallel fast adder using GDI cell. In [11], she discussed an exhaustive analysis and design methodology for commonly used high-speed primitive gates and adder circuit using self-resetting logic. Satish Sharma et. al. in [12] proposed a novel reversible gate and the design of reversible multiplexer using the proposed reversible gate. They claimed that their proposed circuit are more optimized in terms of delay, power supply, power delay product and voltage gain.

Section II represents basic GDI function of different logic gates. In section III, the proposed work has been discussed. Section IV reflects the result of simulation of the proposed work. Section V implements the full adder circuit using MGDI. Section VI presents the implementation of 4-bit parallel binary adder using Dsch38. Section VII concludes the proposed work.

## II. BASIC GDI FUNCTION

The basic GDI cell is like a CMOS inverter where the source/drain of a nMOS is connected to the source/drain of a pMOS and is known as output terminal as shown in Figure 1. Common gate input for both the nMOS and pMOS is termed as G. The source/drain of pMOS is termed as P and the source/drain of nMOS is termed as N. Drain of pMOS is not connected to $V_{DD}$ and source of nMOS is not connected to ground like CMOS inverter. Here, in GDI cell, source of both pMOS and nMOS are connected to two input P and N respectively. Bulks of both pMOS and nMOS are connected to P and N respectively so that it can be arbitrarily biased at contrast with a CMOS inverter.

Table I shows that the simple changes at the inputs N and P, make different logic functions. Most of these functions are complex in CMOS implementation but very simple using GDI technique. Here in this paper, I have considered two functions $F_1$ and $F_2$ which are the complete requirement of the logic families. Function $F_1$ is the only GDI function that can be realized in a standard p-well CMOS process. When N input is at high logic level and P input is at low logic level, the diodes between nMOS and pMOS bulks to Out are directly polarized resulting a short between N and P with static power dissipation [10]. This causes a drawback for OR, AND and MUX implementation in regular CMOS technology with $V_{BS}$ = 0 configuration. This draw back can be reduced if the design is performed in floating-bulk SOI technologies [10]. In that case, a full GDI library can be implemented.

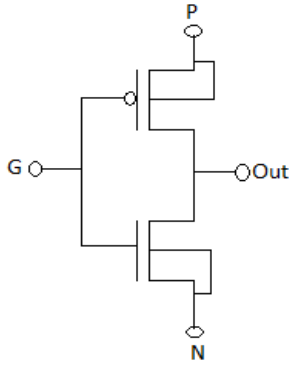



**Figure 1.** Basic GDI cell.

Here the logical functions like AND, OR, NAND, NOR, Ex-OR, Ex-NOR and MUX are being implemented. As an example the operation of OR gate is being elucidated. For OR gate, the drain (P) of pMOS is connected to B, the common gate terminal (G) is connected to A and the source (N) of nMOS is connected to logic high ($V_{DD}$). When both A and B are at logic zero level, pMOS will operate in linear and nMOS is in cut-off. Output (Out) will be according to Shannon expansion theorem, Out = $\bar{A}B + A.1$. Since A = 0, $\bar{A} = 1$, and hence Out = B + A= 0. While A = 1 and B = 0, pMOS is in cut-off and nMOS is in linear and hence Out = 1. While A = 0, B = 1, pMOS will operate in linear and nMOS is in cut-off and Out = 1. While A = B = 1, pMOS will be in cut-off and nMOS is in linear mode and Out = 1.

**Table I.** Various logic functions of GDI cell for different input configurations.

| N | P | G | Out | Function |
|---|---|---|---|---|
| 0 | B | A | $\bar{A}B$ | $F_1$ |
| B | 1 | A | $\bar{A} + B$ | $F_2$ |
| 1 | B | A | A + B | OR |
| B | 0 | A | AB | AND |
| C | B | A | $\bar{A}B + AC$ | MUX |
| 0 | 1 | A | $\bar{A}$ | NOT |

## III. MODIFIED GDI CELL

Modified GDI Cell is a modified version of GDI Cell which is used to design digital circuit with less numbers of transistors hence reducing the area of digital circuits, power dissipation and delay. Its performance is better than CMOS and PTL (Pass Transistor Logic). The bulk of nMOS and pMOS of GDI Cell are connected to ground and $V_{DD}$ respectively as shown in Figure 2.

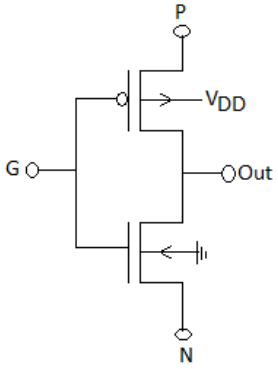



**Figure 2.** Modified GDI Cell.

Figure 3 shows the AND gate using modified GDI Cell. Drain of pMOS is connected with input 1 and with the gate input and the source of nMOS is connected with input 2. When both the inputs are zero, then pMOS will operate in linear mode whereas nMOS is in cut-off resulting output zero. When input 1 is one and input 2 is zero, pMOS is in cut-off and nMOS will operate in linear mode resulting output zero. Similarly when input 1 is one and input 2 is zero, pMOS is in linear mode and nMOS is in cut-off producing zero output. When both the inputs are one, pMOS is in cut-off and nMOS is in linear resulting output one. The four conditions are shown in Figure 4.

The performance analysis made with respect to transistor count, power dissipation and switching delay of MGDI, GDI, CMOS and TG is presented in Table II. From the table, it is clear that GDI Cell requires only two transistor for implementation of AND, OR, NOT and MUX gates. The worst case with respect to transistor count is CMOS MUX. It is also clear from the table that the power dissipation of MUX is larger than any other gate, since the implementation of MUX is complicated and it requires an additional input. On the other hand NOT gate has the lowest power dissipation. With respect to circuit delay, it is observed that GDI and TG provide the smallest switching delay. Switching delay is more for CMOS gates.

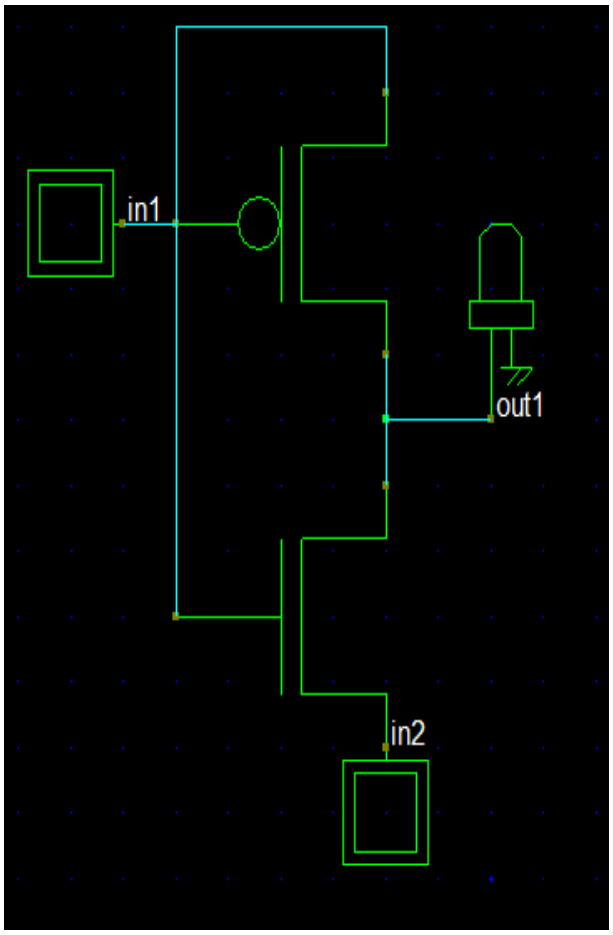
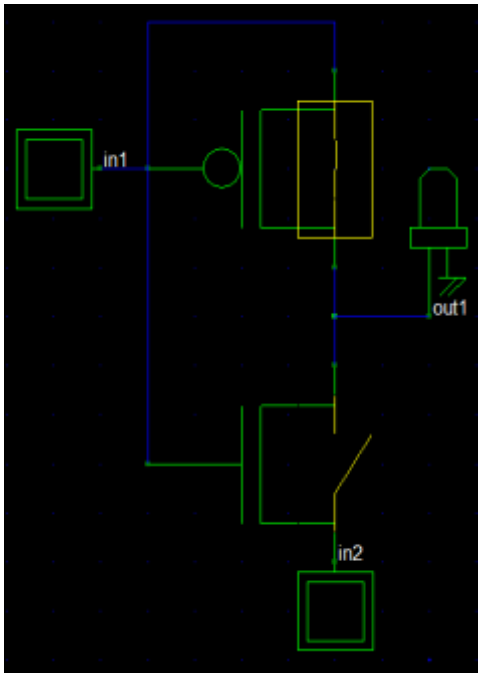
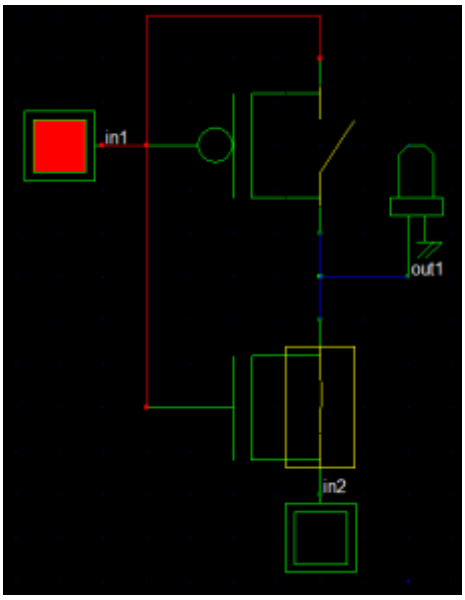


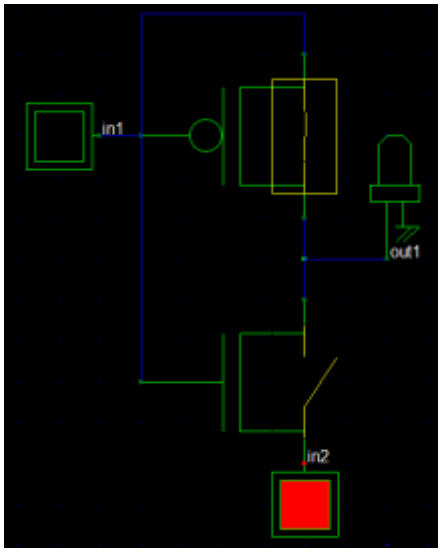

**Figure 3.** Two input AND gate using M-GDI Cell.



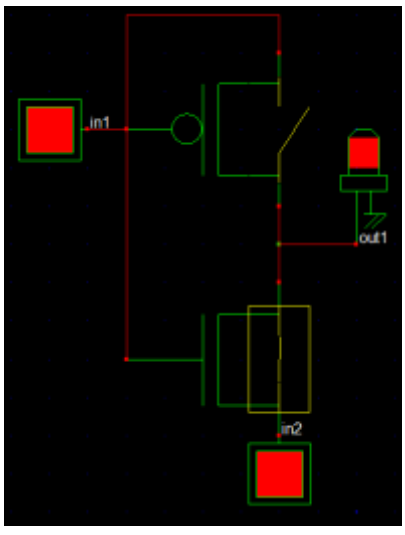

(a) Input1 = input 2 = 0




(b) Input 1 = 1, input 2 = 0




(c) Input 1 = 0, input 2 = 1




(d) Input 1 = input 2 = 1

**Figure 4.** Two input AND gate using M-GDI Cell.

**Table II.** Comparative study of different parameters of different gates.

| Gates | Transistor counts | | | | Power dissipation in µW | | | | Switching delay in ns | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | GDI | MGDI | CMOS | TG | GDI | MGDI | CMOS | TG | GDI | MGDI | CMOS | TG |
| AND | 2 | 2 | 6 | 6 | 1.284 | 0.982 | 1.71 | 1.52 | 0.8 | 0.8 | 1.4 | 0.8 |
| OR | 2 | 2 | 6 | 6 | 1.32 | 1.23 | 1.55 | 1.55 | 0.8 | 0.8 | 1.7 | 1.1 |
| NOT | 2 | 2 | 2 | 2 | 0.61 | 0.52 | 0.66 | 0.9 | 0.8 | 0.8 | 1.4 | 1.1 |
| XOR | 4 | 3 | 12 | 8 | 1.47 | 1.24 | 1.5 | 1.1 | 1.25 | 1.2 | 2.2 | 1.4 |
| XNOR | 4 | 3 | 12 | 8 | 1.46 | 1.25 | 1.6 | 1.2 | 1.25 | 1.2 | 2.2 | 1.4 |
| MUX | 2 | 2 | 8 | 6 | 1.9 | 1.9 | 2.3 | 2.1 | 0.8 | 0.8 | 2.1 | 1.0 |

## IV. IMPLEMENTATION OF XNOR GATE USING GDI CELL

XNOR gate can be implemented using only three transistors as shown in Figure 5. Source of one nMOS and gate of other nMOS are connected to input B. The gate of pMOS, the gate of one nMOS and the source of other nMOS are connected to input A. The drains of the pMOS and the nMOSs are connected to the output C. The Fig. 5 is drawn using Dsch38 lite. Since the number of transistor is less, the propagation delay, the space required and the power dissipation are also small. This diagram is used to implement the diagram of full adder circuit explained in the next section.

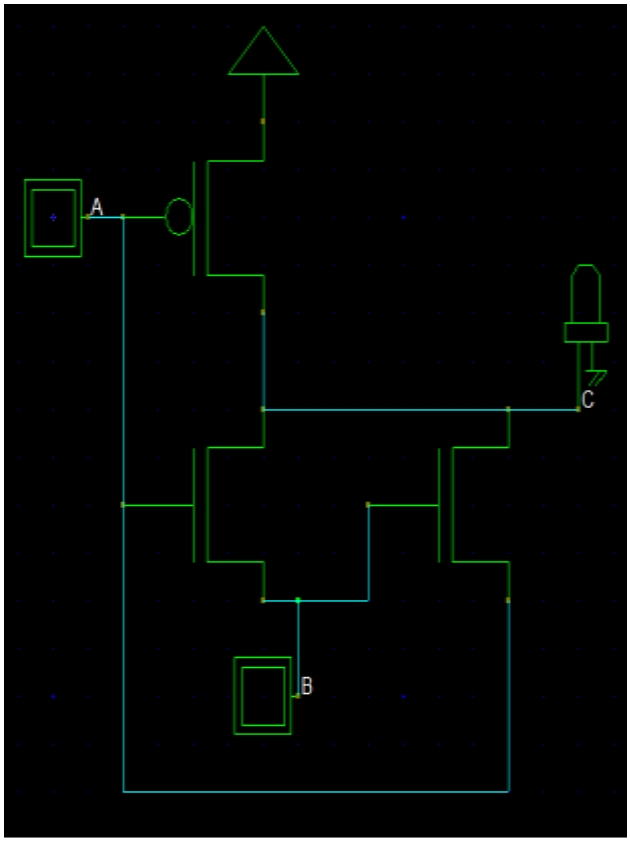



**Figure 5.** XNOR gate using GDI cell.

## V. IMPLEMENTATION OF FULL ADDER CIRCUIT USING GDI CELL

Here one bit full adder is to be implemented using GDI cell. Carry generated for two bits addition namely A plus B is the carry in for the next two bits addition. So the sum for two bits addition is

Sum = A + B + $C_{in}$ (Carry in)

The expression for the sum of two bits and one carry in is

SUM = A⊕B⊕CIN, where ⊕ is the XOR operator. Similarly the expression for Carry out (COUT) is

COUT = AB + (A⊕B)CIN

So two XOR gates and one AND gate are required to implement a single bit full adder circuit as shown in Figure 6.

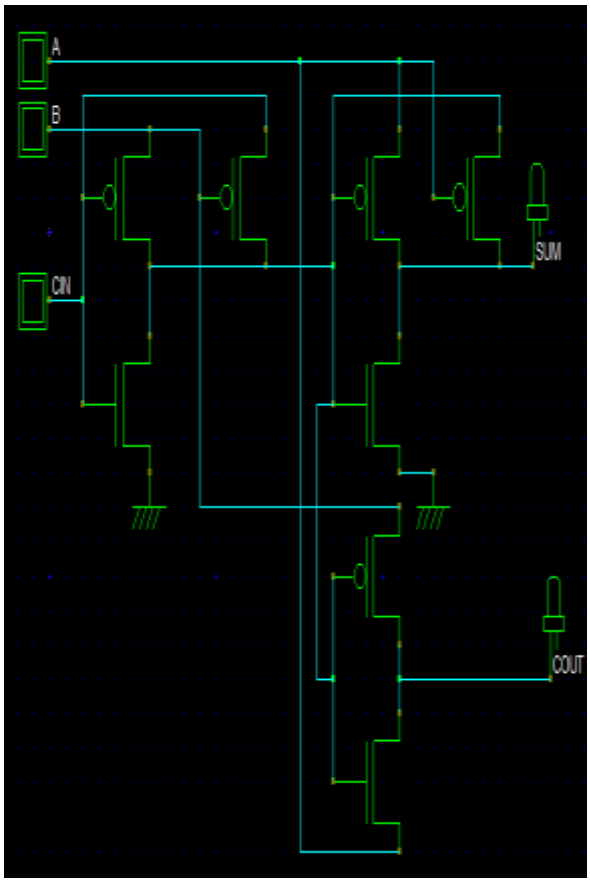


**Figure 6.** Single bit full adder circuit using two XOR and one AND gates.

In the figure A and B are the two bits that will be added with CIN to get SUM and COUT. From the Fig. it is clear that only eight transistors are required to implement a full adder circuit. The timing diagram of the single bit full adder drawn using Dsch38 lite is shown in Figure 7.

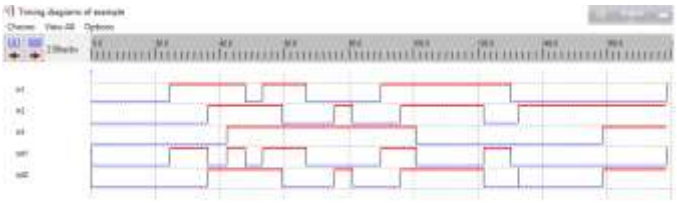


**Figure 7**. Timing diagram of single bit full adder circuit.

Table III shows the comparison of different parameters using different techniques for full adder design. The comparison has been made on the basis of transistor required, power consumption, propagation delay and space required. From the comparison table, it is clear that MGDI is the best technique for full adder implementation with respect to the other techniques mentioned above.

**Table III.** Comparative study of different parameters using different techniques.

| Parameters | CMOS | Transmission Gate | PTL | CPL | GDI | MGDI |
|---|---|---|---|---|---|---|
| Transistor count | 28 | 20 | 28 | 32 | 10 | 8 |
| Propagation delay(ps) | 110.24 | 106.32 | 112.46 | 118.6 | 18.56 | 12.24 |
| Power consumption (watt) | $4.2x10^{-6}$ | $3.9x10^{-6}$ | $4.1x10^{-6}$ | $4.6x10^{-6}$ | $1.9x10^{-7}$ | $1.4x10^{-7}$ |
| Space required ($cm^2$) | $2.9x10^{-5}$ | $1.8x10^{-5}$ | $2.8x10^{-5}$ | $3.14x10^{-5}$ | $1.6x10^{-6}$ | $1.2x10^{-6}$ |

## VI. IMPLEMENTATION OF 4-BIT PARALLEL ADDER

Parallel adder is a combinatorial circuit adding every bit position of the operands in the same time. Thus it is requiring number of bit-adders (full adders + 1 half adder) equal to the number of bits to be added. Suppose $A_4A_3A_2A_1$ (which is a 4-bit stream) is to be added with $B_4B_3B_2B_1$ (which is another 4-bit stream). The addition operation is shown in Figure 8.

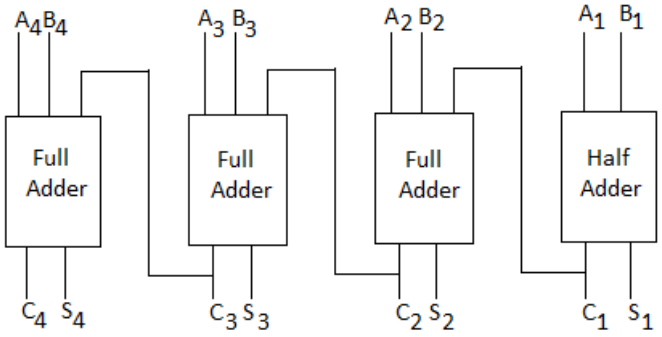



**Figure 8.** 4-bit parallel binary adder.

In fig. 8, $S_4$, $S_3$, $S_2$ and $S_1$ are the sum whereas $C_4$,$C_3$, $C_2$ and $C_1$are the carry output. First adder is a half adder since there is no carry input for this adder. The same block of 4-bit parallel binary adder using Dsch38 lite is shown in Figure 9 and the corresponding timing diagram is shown in Figure 10. A comparative study of the proposed 4-bit adder has been made in table IV with other techniques such as CMOS, PTL, CPL with respect to power consumption, transistor required, propagation delay and space required. From the table, it is clear that MGDI technique is the most advantageous design technique over other techniques.

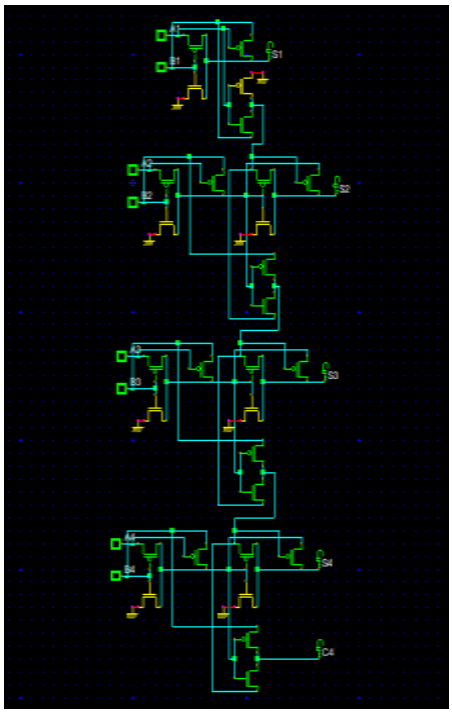


**Figure 9.** 4-bit parallel binary adder using Dsch38 lite.

## VII. CONCLUSION

This paper deals with the advantages of MGDI over GDI, CMOS, PTL, CPL with respect to the transistors count, power consumption, propagation delay. Though an XNOR gate can be implemented using 12 transistors in CMOS technique, this paper includes the presentation of XNOR gate using MGDI technique with less numbers of transistor. This paper also represents how a full adder and 4-bit parallel binary adder circuit can be implemented using MGDI technique for less numbers of transistors. Also the timing diagram of the full adder and 4-bit parallel adder have been explained here using Dsch38 lite.

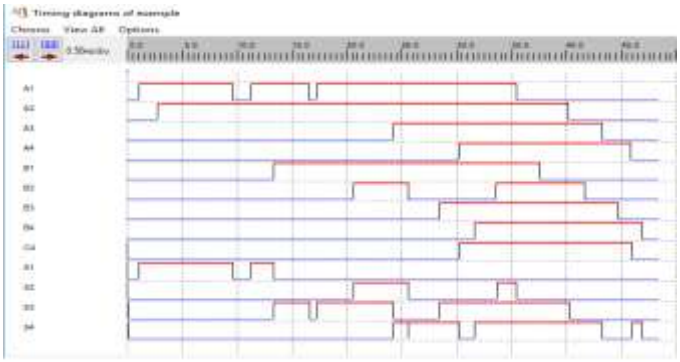


**Figure 10.** Timing diagram of 4-bit parallel binary adder.

**Table IV.** Comparative study of different parameters of MGDI with CMOS, Transmission gate, PTL, CPL and GDI.

| Parameters | CMOS | Transmission gate | PTL | CPL | GDI | MGDI |
|---|---|---|---|---|---|---|
| Transistor count | 94 | 72 | 98 | 108 | 36 | 29 |
| Power consumption(watt) | $15.2x10^{-6}$ | $14.3x10^{-6}$ | $12.2x10^{-6}$ | $13.2x10^{-6}$ | $7.6x10^{-7}$ | $5.2x10^{-7}$ |
| Propagation delay (ps) | 400.25 | 350.46 | 412.36 | 403.67 | 60.46 | 40.12 |
| Space required ($cm^2$) | $10.1x10^{-5}$ | $6.4x10^{-5}$ | $9.4x10^{-5}$ | $11.2x10^{-5}$ | $5.4x10^{-6}$ | $3.9x10^{-6}$ |

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