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High Performance FinFET based Three Stage Operational Amplifier

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Abstract: In this paper, FinFET technology based three stage op-amp. is proposed. The DC gain, bandwidth, input resistance, output resistance and unity gain frequency (UCF) of the proposed FinFET based three stage op-amp are found to be better than conventional CMOS based FinFET based three stage op-amp. Both three stage op-amp were designed at 32nm technology using LTSPICE simulator.

Keywords— FinFET, CMOS-FET, DC Gain, UGF

I. INTRODUCTION

The single stage operational amplifier is a differential pairs that permit the straight pass the small signal currents generated through the input differential pairs across the output impedance. Thus, they limit the gain of their particular topologies that are multiplication of input pair trans-conductance and the output impedance. Although such gain in these circuit could enhanced by the employ of cascade of these circuit, the output fluctuation of such op-amps are else restricted due to adding up of transistor stages. Usually this restriction needs to be assigned as the gain and for voltage fluctuation presented by the cascaded amplifiers are not enough to the desired utilization. While in these case we have alternatives for three stages op-amps it deals along with gain as well as output swing restrictions. However in these configurations usually the first stage generates a large gain and it gives high swing later. These three stage op-amp are hence highly efficient than the cascade op-amp because it isolate and they deal independently with the swing requirement and with gain.

S. Morrison et. al. [1] study a fully differential operational amplifier in FinFET and Planar Technology and show the bulk FinFET as a feasible option to planar bulk technology. With that a new benchmarking proposal is implemented in order to efficiently and relatively compare in simulation. A. Verma et. al. [2] conducted experiment which includes model test of design of two stage CMOS operational amplifier and find out its results according to design parameter. The results of the op-amps shows its drain current, power dissipation, gain of the device, and unity gain frequency and bandwidth of circuit.

E. Contreras et. al. [3] analyzed simulation of miller op-amp analog circuit with FinFET transistor. FinFET transistor used due to continuous decrease in channel length of the transistor and reduction in supply voltage. FinFET transistor op-amp always show challenges during study or simulation. Hence, this study we look at the advantage of FinFET over CMOS. M. Alioto et. al. [4] conducted laboratory study on the assessment of layout density in three terminal, four terminal and multi gate FinFET standard cells. It shows different mode of FinFET operation, explained difference on SOI FinFET and bulk FinFET. M. Agostinelli et. al. [5] investigated leakage delay tradeoff in FinFET logic circuit and completed comparative analysis with bulk technology. A. Amara et. al. [8] performed a layout structure of planar double gate transistor and show how fin hold the source and drain channel three dimensionally on all side and created two gate terminal device. Fin hold very tightly within it and increase gate control over the device. according to that double gate devices are also called as FinFET. The main target t planar double gate mainly focuses on SOI CMOS transistors, fully depleted with double

independent planar gates. L. Selmi et. al. [7] studied DC performance of sub-threshold CMOS logic for ultralow power from the point of view of circuit design. Hence, it gives an useful execution of small signal along with the larger signal models for sub-threshold section operations of MOS transistors J.P Colinge et. al. [9] studied FinFET and other multigate transistor. FinFET devices and other multigate device have advantages over three terminal devices. In conventional devices when channel length become shorter than depletion width then short channel effect occurs. Short channel includes GIDL, hot electron effect, DIBL, impact ionisation, velocity saturation.

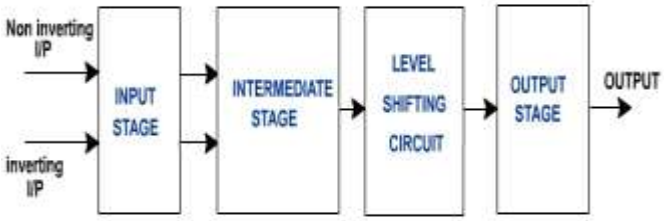

Figure 1 Block diagram of op-amp.

S.No.	FinFET	CMOS
1.	U1 = 58	M1 = 58
2.	U2 = 58	M2 = 58
3.	U3 = 14	M3 = 14
4.	U4 = 18	M4 = 18
5.	U5 = 26	M5 = 26
6.	U6 = 29	M6 = 29
7.	U7 = 29	M7 = 29
8.	U8 = 102	M8 =102
9.	U9 = 05	M9 = 05
10.	U10 = 14	M10 = 14
11.	U11 = 14	M11 = 14

Figure 2. W/L ratio of FinFET and CMOS transistors, used in proposed structure of FinFET and CMOS based three stage operational amplifier.

II. PROPOSED CMOS AND FINFET BASED THREE STAGE OP-AMPS.

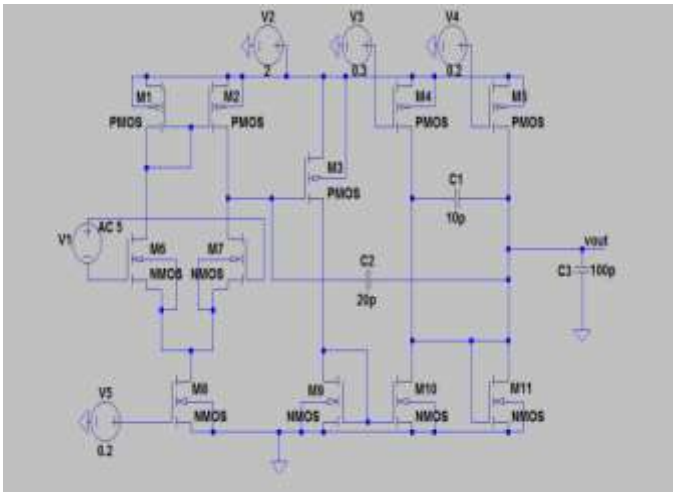

Figure 3. Conventional Schematic of CMOS based three stage op-amp

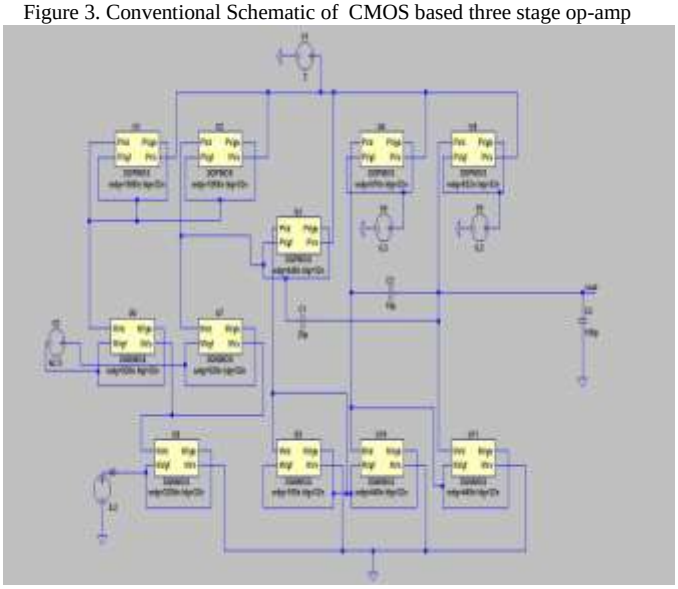

Figure 4. Proposed *FinFET based three stage op-amp*

Figure 3 demonstrates conventional CMOS based three stage op-amp. Figure 4. Proposed FinFET based three stage op-amp This circuit is simulated using LTSPICE at 32nm, with 2V VDD.

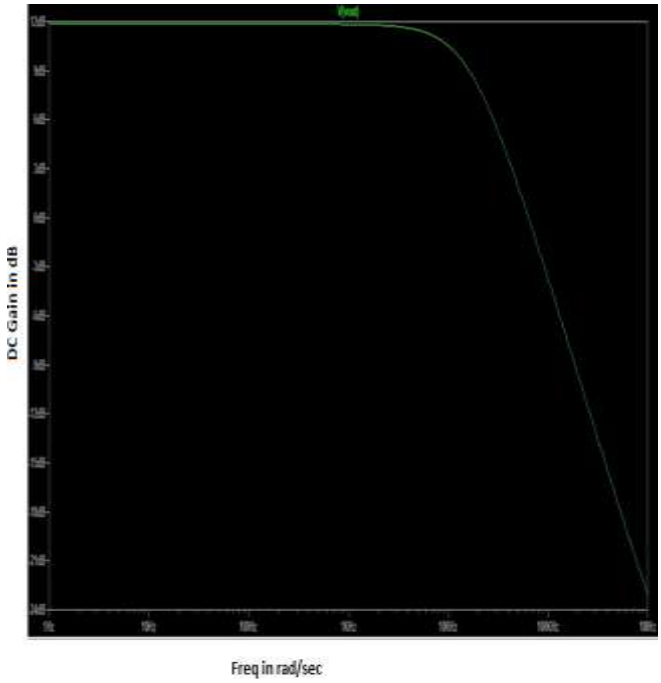

Figure 5. Gain of CMOS based three stage operational amplifier.

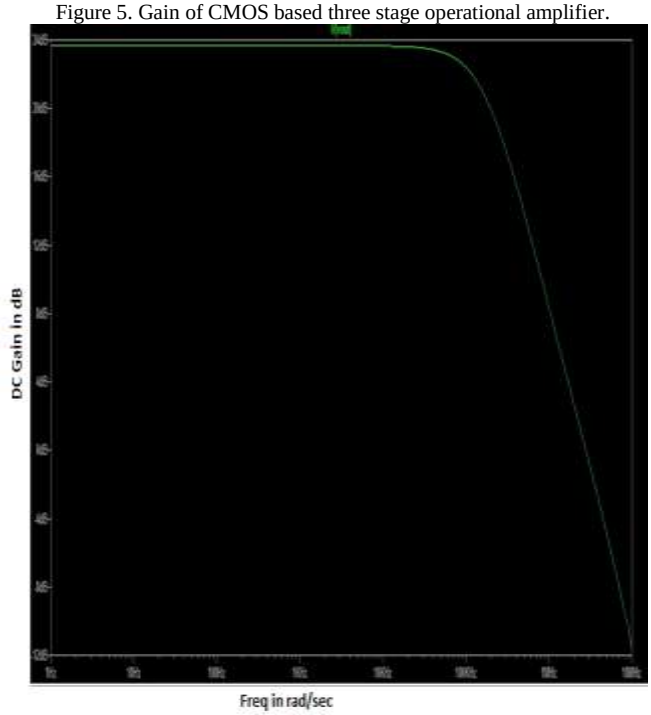

Figure 6. Gain of FinFET based three stage operational amplifier

The proposed CMOS based op amp designed at 2V provides, DC gain of 11.50 dB, bandwidth of 92.53 KHz, input impedance of 4.48×10^{8} ohm and output impedance of 472 ohm . By comparing the proposed design with FinFET based three stage amplifier at same supply voltage it is observed that DC gain comes to be 23.80 dB, bandwidth of 4.01 MHz, input impedance of 3.22×10^{18} ohm, output impedance of 939 ohm.

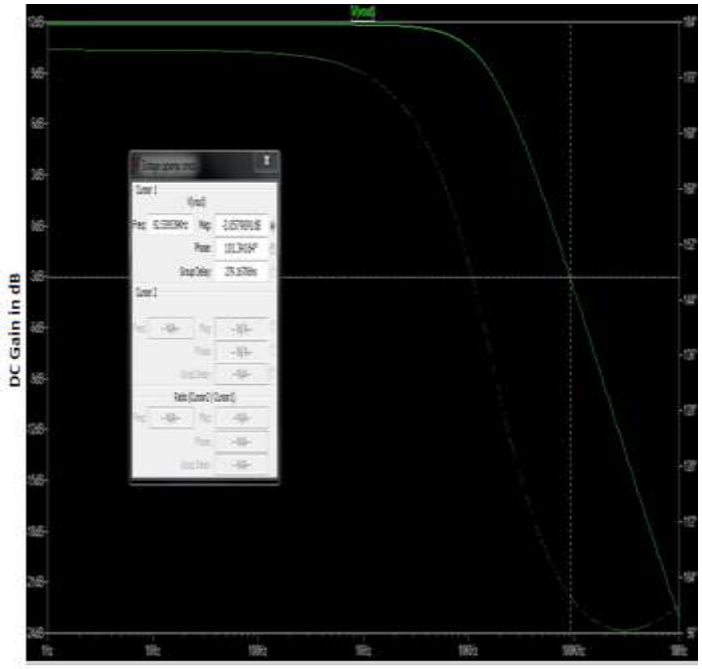

Figure 7. Bandwidth of CMOS based three stage operational amplifier.

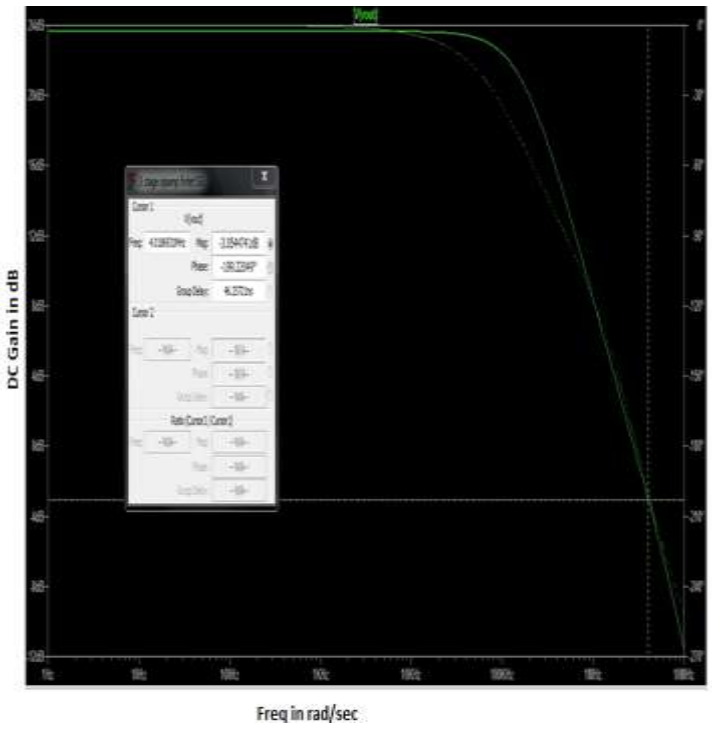

Figure 8. Bandwidth of FinFET based three stage operational amplifier

TABLE 1: Comparative analysis of Comparison results of proposed CMOS based three stage Op-Amp and FinFET based three Stage Op-Amp @ 32 nm tech. node at 2V.

S. No.	Parameters	FinFET based three Stage Op-Amp	CMOS based three stage Op-Amp
1.	**Gain**	23.80 dB	11.50 dB

2.	**Input Resistance**	3.22×10^{18} ohm	4.48×10^{8} ohm
3.	**Output Resistance**	939.35 ohm	472.61 ohm
4.	**Bandwidth**	4.01 MHz	92.53 KHz
5.	**UGF**	2.78 MHz	63.36 KHz

III. CONCLUSION

In this paper, three stage operational amplifier structures are designed and simulated using conventional CMOS and FinFET at 32 nm technology node. In both simulated amplifiers the load capacitance was consider as 100 pF and the compensation capacitors C1 and C2 are 20pF and 10pF respectively, So the 32nm CMOS technology and 32nm FinFET technology are compared using the same design methodology and the same set of specifications.AC and transient analysis are performed to calculate and find the different performance measuring parameters of the proposed three stage operation amplifiers.

Result shows that FinFET technology is able to deliver more gain, better input and output resistance and high bandwidth as compare to conventional CMOS technology three stage operational amplifier. So the proposed FinFET technology can be better alternative to CMOS technology for short channel devices. The gain, bandwidth, input & output resistance, unity gain frequency of the FinFET three stage op-amp are better than CMOS Based.

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