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Low Power VCO Design for Wireless Communication Based Applications

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Abstract: Wireless communication-based system requires low power, current, voltage and wide frequency range for system design. The Paper presents a design in the field of wireless communication systems. It presents 3 stage voltage controlled ring oscillator design on LT Spice tool and also reports transient, DC analysis of the system. As well as it shows fast fourier transform response of input control voltage and its transient analysis response with change in time period and frequency. The proposed design is implemented in 45nm technology and achieved low voltage and current range in table 1. VCO power and current estimation done based on mathematical modeling and compared with simulation results. Authors have also achieved low power dissipation of 37.6 µw, the Phase noise of VCO design from -90 dB to 40 dB with frequency 1 MHz offset frequency and shows DC sweep analysis from 0 to 4.8 volts voltage range for 0 to 0.6 seconds time period.

Keywords: Complementary MOSFET, NMOS, PMOS, FFT, VCO

I. INTRODUCTION

Nowadays very large scale integration based industries are growing rapidly because of advancement in electronics and communication system. Due to recent technologies peoples want to be associated all the time with wireless-based devices. Paper focuses on the design of VCO for such type of applications. This work is based on the controlled oscillator circuit. Two important types of controlled oscillator are useful in electronics industries.

(A) Voltage controlled oscillator with a voltage control signal.

(B) Current controlled oscillator with a current controlled signal.

Our paper focuses on low voltage; current and power based CMOS VCO design for communication-based applications, which plays a very important role in current research. This work appears in many RF signal processing, and mixed signal circuit design. VCO is an electronic device useful for signal generation purpose with definite frequency [1]-[4]. This paper discusses 3 stage VCO design for 45 nm technology, which is useful in data communication, modulation, and demodulation of the signal. These systems are based on incoming data signal with a clock recovery circuit to track clock rate. Its design is based on various parameters like center frequency, tuning range, sensitivity, spectral purity [5]-[8].

II. METHODOLOGY

Figure 1 shows, 3 stage voltage controlled ring oscillator using delay stages. An output of the last stage is going to the input of the first stage. This oscillator is generating periodic or analog signals with a finite frequency range. It is formed using 3 stage inverter circuit with oscillation phenomenon whereas oscillation formed using odd no. of stages. It is the basic condition for DC signal conversion [9], [10]. The ring kind of designing must represent 360^0 and its voltage is also unity for alteration occurrence. π/N phase shift is provided by each delay element. N is representing here the total count of delay devices. The rest π phase shift is delivered by dc inversion of the inverter delay element. The odd number of delay stages are must here for DC inversion of single-ended oscillation circuit.

For VCO circuit design oscillation frequency for N stage would be $F_0 = 1/2Nt_d$, where total delay element is represented by N. Literature survey reported here for various types of delay devices for oscillation circuit, which includes numerous feedback loop, twin delay, and single-ended delays. It has been implemented by various techniques like the latch, cross-coupled cell, and inverter stages. This designing is the very basic building block to design the VCO circuit and improved

design of this delay device can affect the total recital of the whole circuit [11]-[13]. In this reported work a new delay element has been implemented the significance of intake power of overall design, voltage, current, and frequency range.

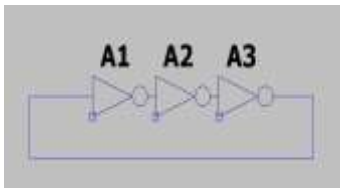

Figure 1 Voltage Controlled Ring Oscillator

Figure 2 shows CMOS VCO design using the current starved method. M4 & M8 are working as an inverter, M1 and M11 are using as a current source which limits the available current on M1 and M8. The MOSFETs M7 and M14 drain current are the same and set as an input control voltage [14], [15]. These two MOSFETs are mirrored in each inverter. Here all PMOS transistors are connected to the gate of M7. All NMOS transistors are taking source voltage as an input voltage.

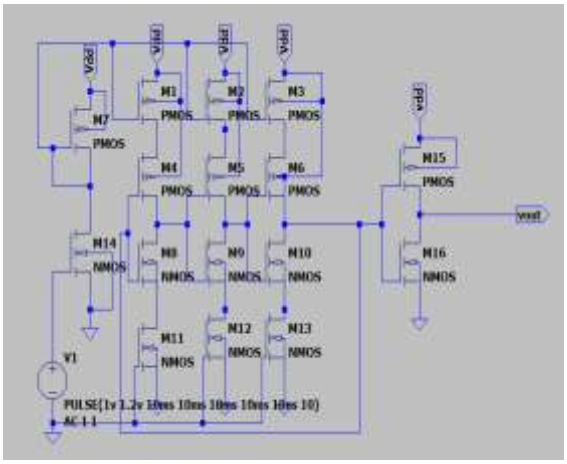

Figure 2 VCO design using a current starved method

III. VCO POWER & CURREN ESTIMATION

The total capacitance on drains of MOSFETs M_4 and M_8 is given by

$$C_{total} = C_o + C_i \quad (1)$$

Where C_{total} the total capacitance on the drain of transconductance, Co is the output capacitance and C_i is the input capacitance. The frequency of oscillation of the current starved 3 stage VCO would be

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N.C_{total}V_{DD}} \quad (2)$$

Here N is the total number of stages and t_1 is output propagation for high to low delay time as well as t_2 is output propagation for low to high delay time [14]. The maximum VCO oscillation frequency Fmax is determined by finding I_D when

$$V_{input} = V_{DD} \quad (3)$$

The average current of VCO depends upon VDD, C_{total} and the number of stages and is given by

$$I_{avg} = \frac{Q_{Ctotal}}{t} = \frac{V_{DD}.C_{total}}{t} \quad (4)$$

Here in eq. (4) Q_{Ctotal} is the charge on C_{total}.
Hence Power dissipation in current starved VCO would be

$$P_{avg} = V_{DD}.I_{avg} = V_{DD}.I_D \quad (5)$$

Where, P_{avg} is average output power of the circuit.

Hence due to design requirements power and current parameter should be low [15], [16]. Due to parameter optimization methods power and current sources may reduce. It is possible by some techniques like:

1) Reduce unwanted circuit from the design for a particular duration.
2) Reduction in input supply voltage.
3) Reduction in low-frequency operation.

These techniques help to reduce power and current parameters in the circuit design.

IV. RESULTS

Figure 3 shows input control voltage from 1 to 1.8 volts at a variable time period, whereas figure 4 shows the FFT response of input control voltage. This analysis is very important in communication and signal processing based systems for accurate calculation of parameters. This response is used for analyzing the input signal in dBm per hertz. It shows various colors in the graph for various values of voltage parameter in each stage of the VCO circuit at a variable frequency. Similarly, figure 5 represents DC sweep analysis under the variable voltage and current range. Transient analysis of the VCO circuit is shown in figure 6 and 7 for variable start and stop time analysis of the circuit. It is used here for calculating the voltage, current and frequency parameters from the circuit.

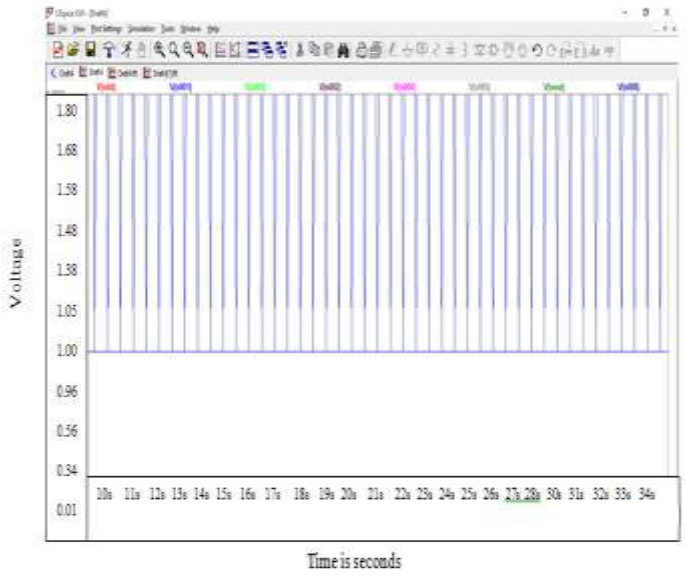

Figure 3 Input control voltages

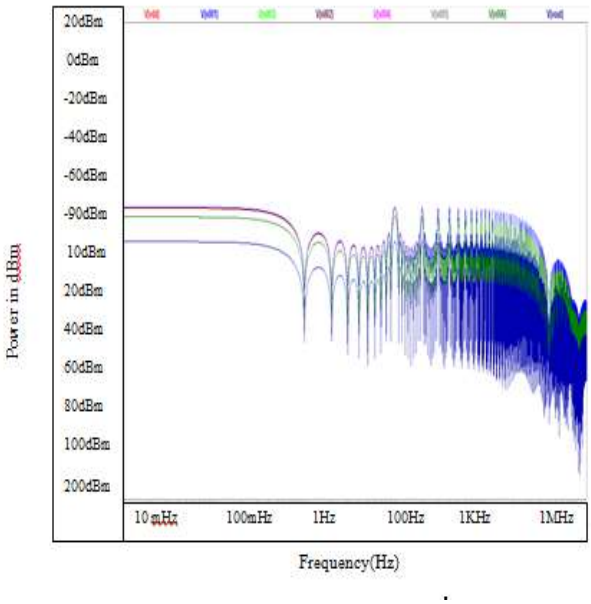

Figure 4 FFT Response of control voltage

Figure 8 shows power spectral density function or noise power of the circuit, in which noise power is varying from -90 dB to + 40 dB with respect to variable frequency range and voltage. Whereas Figure 9 shows voltage versus current graph, which is varying linearly. Voltage is varying from 0 to 10 volts. All nodes of the circuit representing various levels of voltage and current in the circuit.

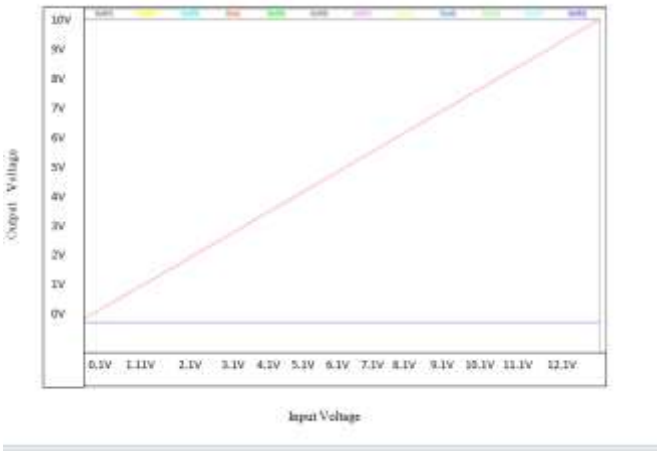

Figure 5 DC Sweep

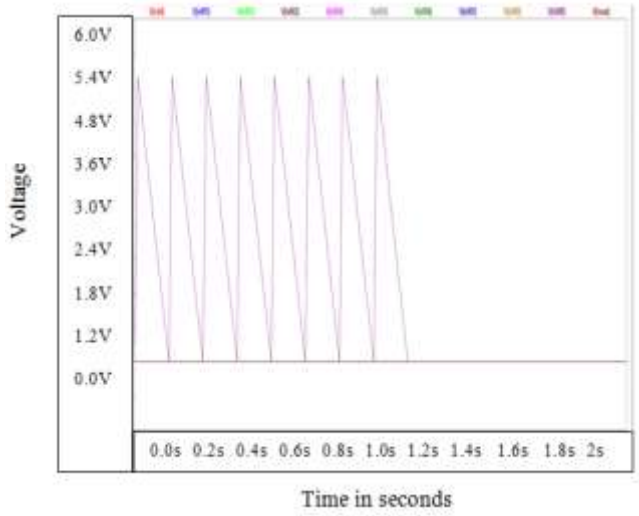

Figure 6 Transient analysis

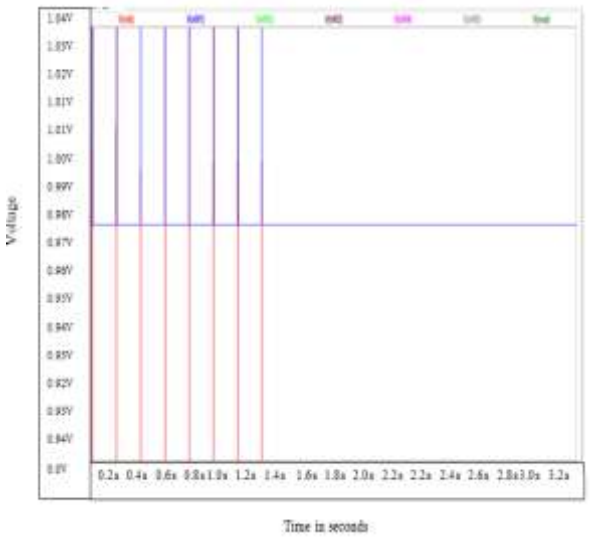

Figure 7 Transient analyses with a change in time period

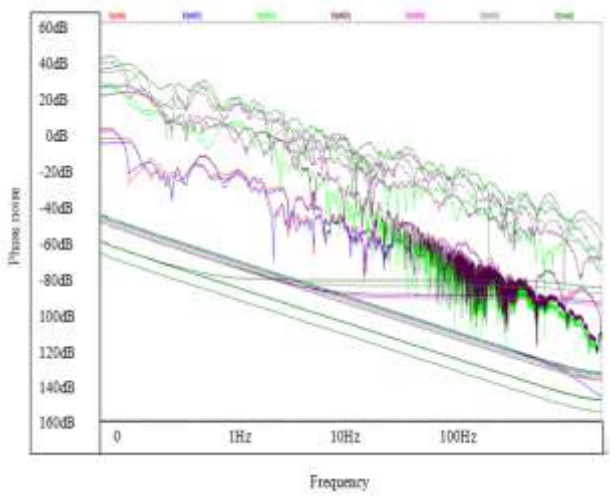

Figure 8 Power Spectral Density Function of Phase Noise

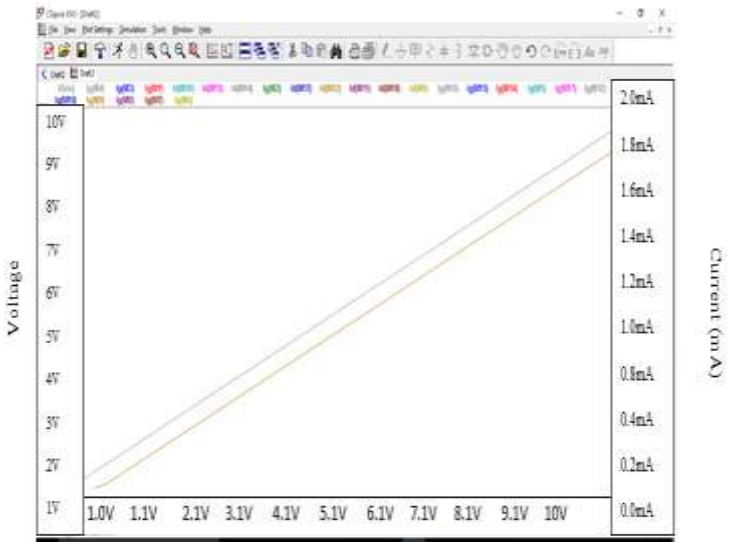

Figure 9 Voltage versus current response of VCO

Table 1 **Comparison of parameters**

Mode	This work	[9]	[11]	[5]
Technology	45 nm	45 nm	90 nm	180nm
Input Control Voltage	1.2	1.5 V	0 .8 V	1.8 V
Nominal Frequency (GHz)	2.58 GHz	1.69GHz	2.54 GHz	1.96-2.4GHz
PSD of VCO phase noise @ 1 MHz offset Frequency	- 90 to +40dB/Hz	----	----	-80.84 dB/Hz
Current Consumption	4µA	----	----	----
Desired Frequency	2 GHz	100MHz	2GHz	2 GHz
Power Dissipation	37.6 µw	50 µw	-----	335.307 µw

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V. CONCLUSION

Paper has been presented low power, voltage and current of VCO design in a wide range of frequencies for the latest research fields of communication, wireless network, and mobile communication systems. Implementation of 3 stages VCO has been done on EDA tool; LT Spice for 45nm technology and also discussed the comparative analysis of various parameters for CMOS technologies.
Whereas phase noise would be -90dB @ 1MHz offset frequency.

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BIOGRAPHIES

Alpana Deshmukh received her Bachelors of Engineering in Electronic & Telecommunication from the SGSITS Indore, R.G.P.V. Bhopal University Madhya Pradesh India in 2004 and M.E. in Digital Instrumentation Engineering from the IET, DAVV University Madhya Pradesh, Indore, India, in 2007. She joined the Department of Electronics and Instrumentation Engineering, DAVV, as a Teaching Assistant in 2005, and in 2008 G. H. Raisoni Institute of Engg. & Technology, Wagholi, Pune as Lecturer where she became an Assistant Professor in 2010. She is currently pursuing Ph.D. from SGSITS, Indore. Her current research interests include testing of mixed signal circuit design, Embedded Processor, Circuit theory and devices, Image Processing. She is a life member of the ISTE.

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