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CURRENT MODE THRESHOLD LOGIC DESIGN

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Abstract: Current mode threshold logic is a popular CMOS based approach to implement logic functions. This paper presents the implementation of logic function using all current mode threshold logic based circuit. It shows logic function can be implemented using CMOS based current mode logic with less transistors. In this paper we are using all current mode circuits consist of two parts: the differential part and the sensor part. The number of transistors in the sensor part is constant and does not depend on the implemented function. The result shows that many functions can be implemented using these predefine circuit and hardware requirement is reduced compared to traditional CMOS based design.

Keywords: Logic Gates, Threshold Logic, Threshold Logic Design, Current Mode Threshold Logic

I. INTRODUCTION

For the near future, we need a promising candidate for digital circuits due to parameter scaling is going down. Threshold logic gates is a candidate for future digital circuit who exhibit less delay, power dissipation and area. A basic threshold logic gates consist of some inputs with some weighted value for eachinput and a threshold weight. The total sum of theinput weights is compared with the threshold weight. If input weights sum is greater than or equal to the threshold weight then digital output show logic 1 (high) otherwise it shows logic 0 (low).

$$f(x1,x2\ldots\ldots xn) = \begin{cases} 1 & if \ \sum_{i=1}^{n} wi.xi \geq wT \\ 0 & otherwise \end{cases}$$

where*wi*is the weight of the ith input, *xi* , *i*= 1, 2…….,n are binary input variable and *wT* is threshold weight for the function *f* . The function *f* is representing the output of the threshold logic gate.

Function which can be implemented using threshold logic gate call threshold logic function (TF). Threshold function implementations using threshold gate circuit consist of two- part, First part isthe differential part and the other one is the sensor part. Differential part consist of two input network: one input network have positive weights of inputs and other one input network have threshold weight and negative input weights. The sensor part gives output by comparing both the input network. The logic networkappears on thepath from Vdd to the output node. By modulatingthe current that charges the output node, theoutput to the correct value. This increases the sensitivity of the logic gate and provides it with the capability to sense thesmall difference incurrents. In latched domino circuits, the logic network consists of nMOS transistors with full input swingsso we used pMOStransistors inthelogic network which can also work on small voltage swings.

In this paper, we show the implementation of threshold logic function using integer weights in all three current mode threshold logic circuit and compare them in power dissipation and delay of logic function implementation.

This paper is organized as follows. Section II presents the working of current mode circuits using an example of threshold function. Section III presents the results of current mode circuits and their power dissipation and delay results. Section IV consists conclusion.

II. CURRENT MODE THRESHOLD CIRCUITS IMPLEMENTATION

Threshold gates are based on threshold decision principle, which means that the output value depends on whether the arithmetic sum of values of its inputs is greater than a threshold. The threshold principle is general itself and conventional simple logic gates, such as AND and OR gates, are special cases of threshold gates. The power of the threshold gate design is to implementation of complex functions using such gates, which allow system realizations that require less number of transistors or gate levels than a design with standard logic gates. Nowadays, there is an increasing interest in threshold logic because a number of theoretical results show that multinomialsize, bounded level networks of threshold gates can implement functions that require unbounded level networks of standard logic gates. Any conventional logic gates can be realize using threshold logic gate circuits.

Example NAND gate implementation using threshold logic .

Table1. F= (x1.x2)'

		Weighted sum	output

x1	x2	-x1-x2	y
0	0	0	1
0	1	-1	1
1	0	-1	1
1	1	-2	0

Now, table 1 is an example, show a threshold gate implementation with the input weights -1 and -1 and the threshold of -1.5.
this implements NAND, x1 and x2 are the inputs so, there can be four combinations 0 0, 0 1, 1 0 and 1 1. And here what is the weighted sum -1-1 so, the weighted sum is $-x\ 1-x\ 2$. So, if you just calculate the weighted sum on these it will be 0, -1 ,-1 and -2. So, in this case, you see -1.5 the first three they are greater than -1.5 ,-2 is less than -1.5 . So, for the first three, the output will be one this, the output will be 0, this is nothing but the NAND function right. So, we have proved that usingthreshold gate we can construct a NAND gate so, therefore, it is functionally complete ok.

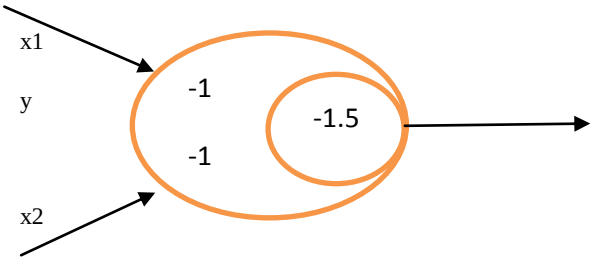

Figure1.TLG for a given weight configuration and input pattern.

Design of logic function*f*using current mode designshow below using three different current mode logic circuits.
Function*f*is $f(x1, x2, x3) = x1'x3 + x2$

Table2. F= (-x1+2 x2+ x3)

			Weighted sum	**output**
x1	x2	x3	-x1+2x2+x3	y
0	0	0	0	0
0	0	1	1	1
0	1	0	2	1
0	1	1	3	1
1	0	0	-1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	2	1

function f (x1, x2 ,x3) with weight configuration (w1 ,w2 ,w3 : wT) where wT is threshold weight and w1 ,w2 and w3 weights belong to x1 , x2 and x3. A possible configure weights is (-1 , 2 , 1 : 0.5) . When we applying the input pattern (x1 , x2 , x3) = (1, 0 , 0) the weighted sum input is -1.0 + 2.0 +1.0 < 0.5 according this output is logic 0 (logic low) and we applying the input (0, 1, 0) then weighted sum is -1.0 + 2.1 + 1.0 > 0.5 this gives logic 1 (logic high).

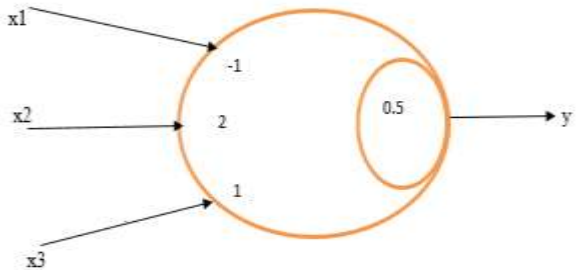

Figure2.TLG for a given weight configuration and input pattern.

A. Current mode threshold logic design (CMTL)

CMTL circuit consists of sensor part and differential part sensor part sense difference between current and differential part is the input part which is subdivided into the threshold part and input part. The threshold consists ofpMOS transistors that implement threshold weight and negative input weights and the input part consist of positive input weights. In CMTL circuit sensor part have three pMOS (p1,p2 and p3) transistors and four nMOS (n1, n2, n3 and n4) transistors. The circuit consists of two types of current *(It)* threshold current and (*In*) active current. Threshold current*It* is total current flowing from threshold part and active current*In* is total current flowing from input part and sensor part sense difference between these two current and change the voltage level of node *op* and node *opb* side according to these current in the circuit. Threshold part which has threshold weight pMOS gate always work active (on) transistor and other pMOS that is negative input and positive input transistors assigned a logic value according to logic. Node *op* and *opb* are output node.

In below circuit fig.3 have x1 and xTpMOS transistors in threshold part and the input part consists of x2 and x3 pMOS transistors with particular weight multiple. Thecircuit consists of single clk which help to operate sensor part and differential part. The operation divides into two part that is the equalization phase and evaluation phase. In equalization phase,clk operates high andtransistorsnMOS n3 and n4 is on because of this value of node M1 and node M2 point same voltage and node *op* and node*opb* also have same voltage at equalization phase. In the equalization phase, p1is off because of this differential, part is not operated. In the evaluation phase,clk goes low because of this nMOS n3 and n4 is off and pMOS p1 is working (on state). When clk goes differential part come in picture and current (*In*) active current and (*It*) threshold start to flow fromthe input part and threshold part. In evaluation phase sensor start working. When we assigned particular weights to inputs and threshold transistors because of this both currents *(In* and *It*)have some difference. If during the evaluation phase the active current (*In*)is greaterthen the threshold current because of this voltage at node *ob* rise faster then voltage at node *opb* and this situation give logic 1 at output and if threshold current *It* is greater then active current *In*then voltage at node *opb* start to rise faster then voltage at node *op* and this situation gives logic 0 at output.

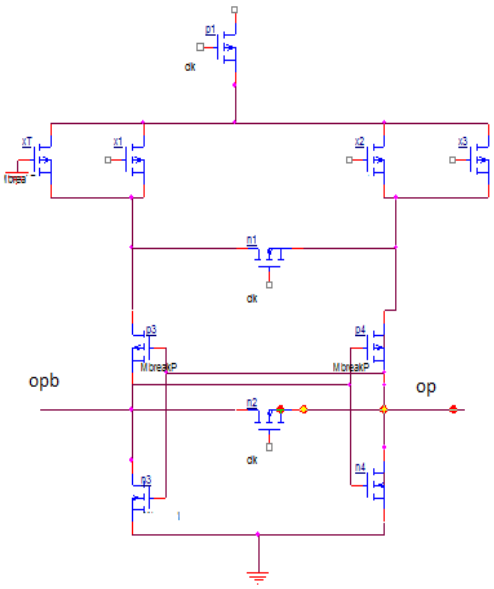

Figure3. Current mode threshold logic design .

B. Differential current mode threshold logic design

Differential current mode threshold logic (DCML) is one of another approach to implementation of the logic function. It also divided into the differential part and sensor part. It has the same working as the earlier circuit of CMTL. In DCML sensor part consist p1 to p4 pMOS transistors and nMOS transistors n1 to n6. In DCML differential part is further divided into threshold part and input part. Threshold current (*It*) flow form threshold part and Active current flow from the input part. Threshold part consist threshold weight pMOS and negative input weights and the input part consist of positive input weights pMOS. Node *op* and *opb* are output node.

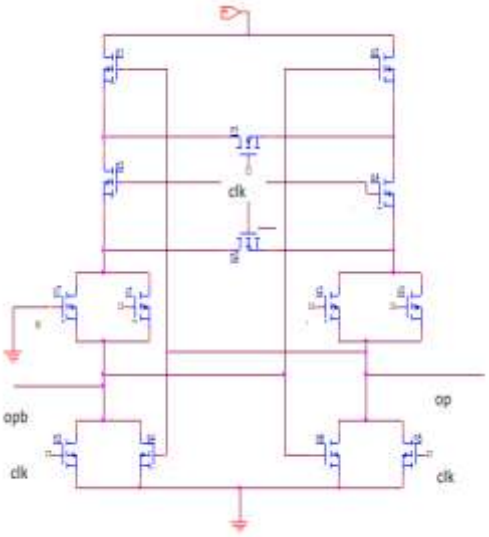

Figure4. Differential current mode threshold logic .

In the above circuit fig. 4 threshold part have x1 and xTpMOS transistors and input part have x2 and x3 positive input weights pMOS transistors. Threshold weight pMOS transistor always work active (on) pMOS transistor and x1, x2 and x3 input pMOS transistors value assigned according to logic. DCML circuit consists of single clk. The operation in DCML is divided into two phases, the equalization phase and the evaluation phase. Sensor part senses the difference in the evaluation phase. When the clk is high equalization phase start working. In equalization phase transistor n1, n2, n3 and n6 are active (on) because of n1 and n2 node voltage at M1 and M2 is equal. When clk is high node *op* and *opb* is connect to the ground. When clk goes low evaluation phase come in picture and differential part start working and the sensor part sense difference between the voltage of node *op* and *opb*. The difference at node *op* and *opb* come because of current It and In. When we assigned particular weights to inputs and threshold transistors because of this both currents (In and It) have some difference. If during the evaluation phase the active current (In) is greater then the threshold current because of this voltage at node op rise faster then voltage at node *opb* and this situation give logic 1 at output and if threshold current It is greater then active current In then voltage at node *opb* start to rise faster then voltage at node op and this situation gives logic 0 at output. In DCMTL

C. Dual clock current mode threshold logic design

Dual clock current mode threshold logic (DCCMTL) is the latest approach to implementation of the logic function. As its name, it consists of two clocks. These clocks used to achieve high speed and low power consumption. DCCMTL is also divided into the differential part and sensor part. In DCCMTL differential part further divided into positive input weights and negative input threshold weight in one side and in other side it consists positive threshold weight and negative input weights as is in below fig. 3. Sensor part consists of six pMOS transistors p1 to p6 and three nMOS transistors n1 to n3. As earlier told DCCMTL consists of two clk, clk1 connected to transistors p1 and n1 and clk2 connected to transistors p5, p6 and p2 as shown in fig. 5. The transistor who contain threshold weight is always active (on). Node op and *opb* are the output node.

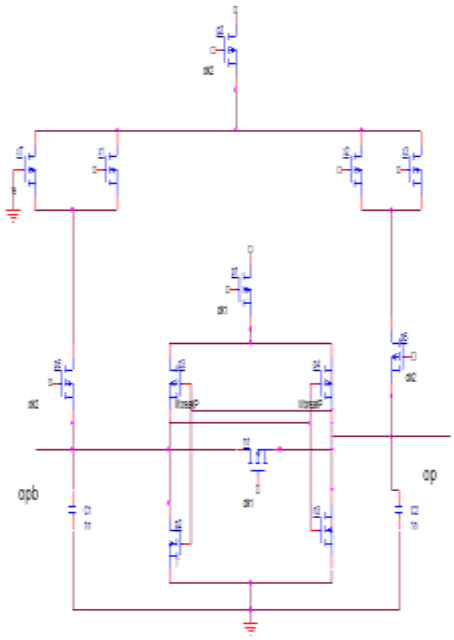

Figure5. Dual clock current mode threshold logic .

In the above fig.5 is the circuit of DCCMTL. In differential part have three blocks first is positive input weights it consists of x2 and x3 input pMOS transistors. Second and third block has negative weight input x1 and positive threshold logic weight xT.The operation of DCCMTL is divided into three phases that are the equalization phase, the pre-evaluation phase and the final evaluation phase . When clocks, clk1 and clk2 are logic (high logic 1) then the circuit is in the equalization phase. In the equalization phase, the voltage at node *op* and *opb* are the same. Node *op* and *opb* directly connected to discharge path in equalization. In the equalization phase differential part not work because of pMOS p5 and p6 and p2 are off. When clk 1 and clk2 are become low (logic 0) then circuit comes in the pre-evaluation phase. In the pre-evaluation phase sensor part and differential part connected to each other by pMOS transistors p5 and p6. When clocks become low pMOS transistors p5, p6, p1 and p2 are become active (on). In the final evaluation phase, clk1 is low and clk2 is active high . In DCCMTL clk2 restrict the current flow from differential block to sensor block, once the voltage difference is established at the output nodes , in this way clk2 help to stop current flowing from differential part to sensor part. This help to minimize power consumption in the circuit.

III. SIMULATION RESULTS

This section presents the simulation results of the proposed current mode circuits in section II. All the circuits implemented in 45nm technology using cadence H spice and out of all circuits shows in the form of waveforms. All the pMOS used in sensor part have width of 240nm. Voltage for the circuits was set to 1.2v as high and 0 as low and the clocks was the same as the voltage. We show power dissipation and delay in the below table . All the waveform shows for the inputs (0,1,0) and (1,0,0) logic. When we used input (0,1,0) it's give output 1 (logic high) and when we used the input (1,0,0) it's give output logic 0 (logic low) .

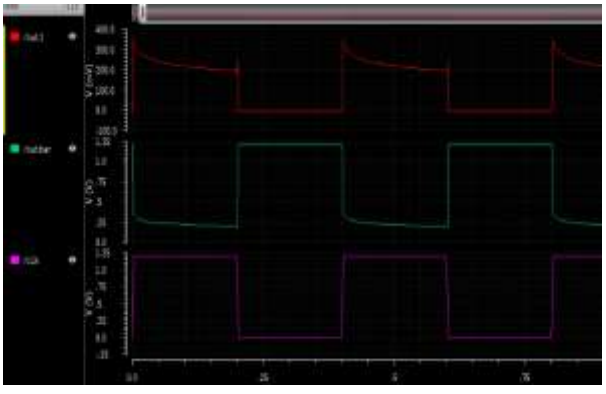

Figure6. Output logic 0 waveform for CMTL circuit .

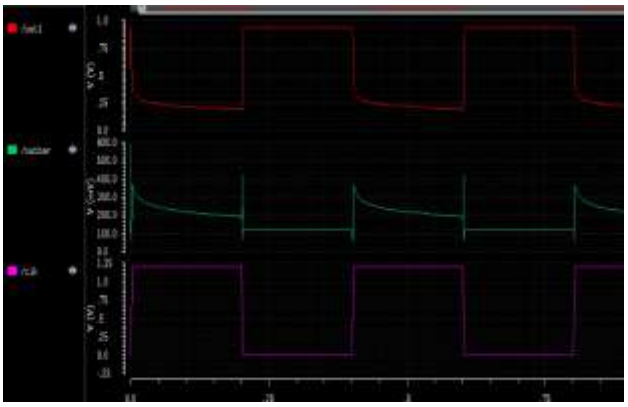

Figure7. Output logic 1 waveform for CMTL circuit

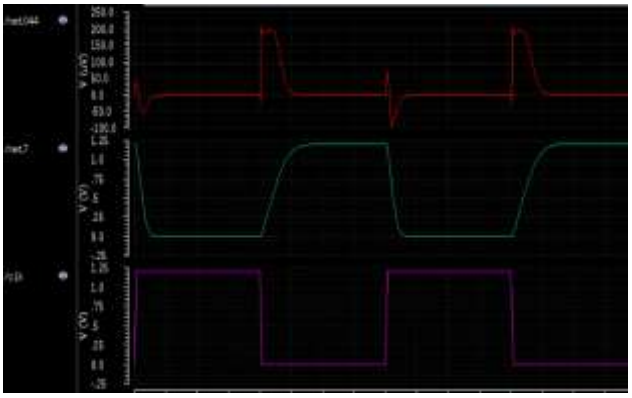

Figure8. Output logic 0 waveform for DCMTL circuit .

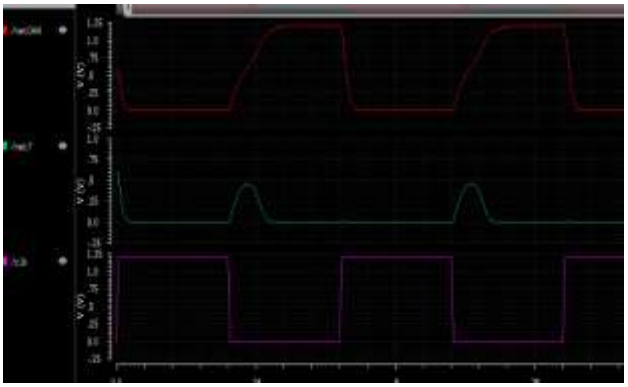

Figure9. Output logic 1 waveform for DCMTL circuit .

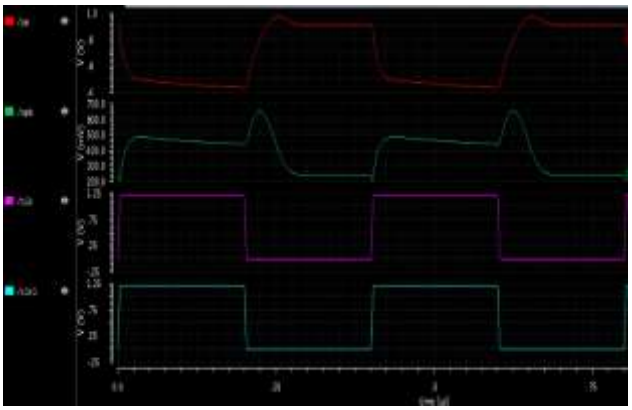

Figure10. Output logic1 waveform for DCCMTL circuit .

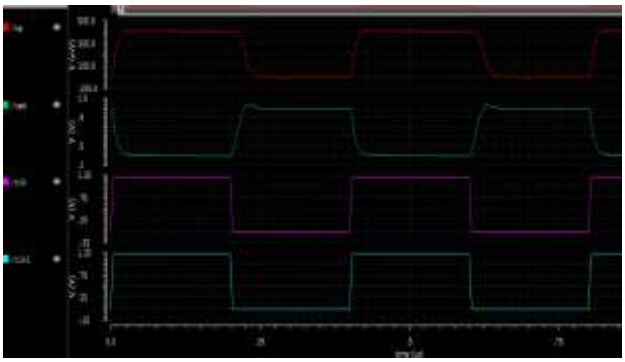

Figure11. Output logic 0 waveform for DCCMTL circuit .

Table3. Simulation results: power dissipation and propagation delay of all circuits

CMTL	Propagation delay(ns)	Power dissipation (uw)
Out 0	.3285	.01264
Out1	.5818	8.673
DCMTL		
Out 0	16.215	4.03
Out 1	20.137	5.95
DCCMTL		
Out 0	14.223	11.12
Out 1	11.163	15.98

Above table shows propagation delay and power dissipation values for the logic (x1'x3+x2). We can see from the above table that for less number of inputs CMTL is a good circuit to use but as we know that DCCMTL circuit have more CMOS component than other circuits so it has more static power dissipation compare to other circuits so for less number of inputs it is not useful benefit of DCCMTL is when we use a large number of inputs because in DCCMTL circuit has duel clock so it shows less dynamic power dissipation.

IV. CONCLUSION

We show a logic function implementation on current mode threshold logic circuits and using these result we can say that for less number of inputs CMTL circuit is good but for a large number of inputs, we can use DCCMTL circuit.Nowadays we are using ultra-deep submicron technology and in UDSM technologyCMOS shows some problem so we can use other device (FINFET , Tunnel MOS , Carbon-Based FET) to replace CMOS. Our future work will implement a large number of inputs function with latest FINFETtechnology .

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