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Capacitance Sizing of CMOS VLSI Circuit in 90nm Technology

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ramanaiah.m@gmail.com**bstract:**

The initial phases of analysis and development efforts in VLSI design were familiarized towards achieving high speed and miniaturization. At present, the growing trends in transportable computing and wireless applications demand the necessity to hunt out new technologies and style circuits that consume low power. This necessitates the necessity to orient the research towards reducing power dissipation in VLSI circuits. Recent trends within the growth and development of battery powered portable and mobile computing devices necessitate the necessity for extended battery life and thence lesser battery power consumption. The battery life is more reduced by the employment of high speed processors and huge recollections in them. Also, the magnitude of power dissipation per unit space within the integrated circuits of gift day microprocessors and recollections square measure chop-chop increasing due to the accumulated speed and flexibility. It is observed from the Table 3,Table4 and Table 5. Proposed CMOS 2 inputs and 4 outputs Decoder, We have compared capacitance sizing like (50fF and 10fF) in condition of power ,delay and area. We have reduced Capacitance Sizing like (50fF and 10fF), 74% Dynamic Power Reduced and 11% delay reduce and 74% Area Reduced in Cadence 90nm Technology.

Keywords: CMOS 2:4 Decoder, high speed, low power and Low area, VLSI, DSP

I. INTRODUCTION

The initial phases of analysis and development efforts in VLSI design were familiarized towards achieving high speed and miniaturization [1]. At present, the growing trends in transportable computing and wireless applications demand the necessity to hunt out new technologies and style circuits that consume low power [2]. This necessitates the necessity to orient the research towards reducing power dissipation in VLSI circuits. Recent trends within the growth and development of battery powered portable and mobile computing devices necessitate the necessity for extended battery life and thence lesser battery power consumption[3]. The battery life is more reduced by the employment of high speed processors and huge recollections in them. Also, the magnitude of power dissipation per unit space within the integrated circuits of gift day microprocessors and recollections square measure chop-chop increasing due to the accumulated speed and flexibility. This worsens the matter of warmth removal and cooling (Kaushik Roy 2000). Also, these high power densities reduce chip dependability and anticipation, increase cooling prices and will even cause environmental problems in giant knowledge centers. Escape power is additionally increasing with technology scaling and can't be neglected. of these factors demand the necessity for value effective solutions to power problems; else improvements in chip technology can reach a standstill [4].

In this work is designed as pursue category II today Literature survey on CMOS 2inputs and 4 outputs Decoder Category III today the methodology for CMOS 2inputs and 4 outputs Decoder and also discussed the High speed, low power and low area. Category IV shows the simulation results explained clearly, after the work is concluded with category V.

II. LITERATURE SURVEY

Power aware techniques are devised in the least levels of the system style like circuit level, device level and beaux

arts level (Unsal and Koren 2003)[5].The power consumption of the multiplier factor unit has been found to be directly proportional to the amount of change activities within the unit. the ability consumption may be significantly reduced by reducing the switching activities. the most functions of a multiplier factor ar partial product generation and summation[6]. thus the researchers have targeted on the look of multipliers to cut back the number of power consumption by reducing the partial merchandise[7]. this could be achieved by reducing the change activities of the multiplier factor. This has driven the analysis to research the change activities of high speed low power multipliers and implement for varied applications[8]. thus the look of low power multiplier factor considering the hybrid encoding technique is conferred during this thesis with additional analysis. The MACK Associate in Nursingd FIR filter units contains multipliers and an accumulator that contains the add of the previous consecutive merchandise[9]. Therefore, the look of low power MACK and FIR filter concentrates on each multiplier style and adder style. This thesis presents the high level optimization techniques for low power multiplier factor that is employed in low power MAC and FIR filter[10]. The high level techniques talk over with algorithmic program and architecture level techniques that take into account multiplication's arithmetic options and computer file patterns. this is often expected to outmatch compared to the low level optimization[11]. Specifically, it considers the optimization of multiplier factor power consumption by reducing the change activity exploitation the developed encoding algorithmic program. The multiplier factor with the developed cryptography algorithmic program and adder may be used for low power MACK unit and FIR filter[12].

2.1 Techniques for Low Power Design

The 3 degrees of decisions specifically voltage, physical capacitance and activity are projected to form the low power style. The power consumption is optimized by dominant any of the alternatives. However, these parameters don't seem to be utterly orthogonal and can't be optimized independently. This category shortly discusses every of the factors, describing their relative importance, still because the interactions that complicate the ability optimization method[13].

2.2 Voltage

One of the simpler and wide used strategies for power aware computing is dynamic voltage scaling (Ernst et al 2003). Voltage reduction offers the foremost direct and dramatic means that of minimizing power consumption with its quadratic relationship to power. Krishna and Lee (2003) have reportable that an element of 2 reductions in provide voltage yields an element of 4 decreases in energy while not requiring any special circuits or technology[14]. This power reduction is practiced not solely in one a part of the circuit, however within the entire style. The low installation designers ar typically willing to sacrifice exaggerated physical capacitance gate activity for reduced voltage. however provide voltage cannot be ablated on the far side some level as a result of apart from power, many factors ar expected to regulate the choice of a system provide voltage. the first issue is performance necessities as provide voltage is down, circuit delays increase linearly[15].

2.3 Physical capacitance

Dynamic power consumption is directly proportional to physical capacitance being switched (Bakoglu 1990, Yeap 1998). thence reduction in power consumption are often achieved by minimizing the shift capacitance. the first sources of the physical capacitance in CMOS circuits ar device and interconnect. the most contributions come back from the gate and junction capacitances and therefore the quantity of capacitance unbroken at a minimum level victimization tiny devices and short wires. It's additionally terribly troublesome to optimize capacitance severally as a result of reducing the scale of the device not solely reduces the physical capacitance however additionally reduces this driving capacity of the semiconductor device[16]. This reduction within the current drive can build the circuit operate terribly slow. So, the researchers contemplate the aspect effects whereas minimizing the physical capacitance[17].

III. DESIGN METHODOLOGY

3.1 Decoder

Instructions similarly as numbers square measure reborn by suggests that of pulsation line in digital system or binary levels. The decoder found a selected cipher. The N inputs whatever may be a high or a low, thus for a certain there are 2N 2 input composition. Because everyone input combo only one of the M outputs are operating that is one and every one alternative outputs can stay operating that is zero. A cryptographer could be a circuit that reversal a code into a group of knowledge. Interest known as a cryptographer as a result of it will the reverse method of encoder. There are numerous cryptographer conferred until these days however here we'll style a 2inputs and 4 outputs decoder with the assistance of NAND circuit[18].

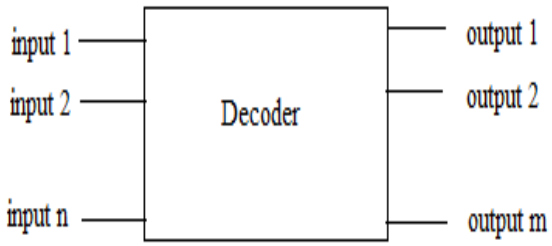

Figure. 1 N Inputs and M Outputs decoder .

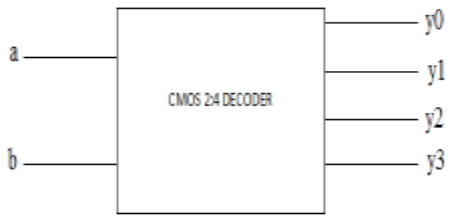

Figure 2: proposed CMOS 2 inputs and 4 outputs Decoder

Table 1: Truth table of CMOS 2inputs and 4 outputs decoder.

Inputs			Outputs		
a	b	y0	y1	y2	y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

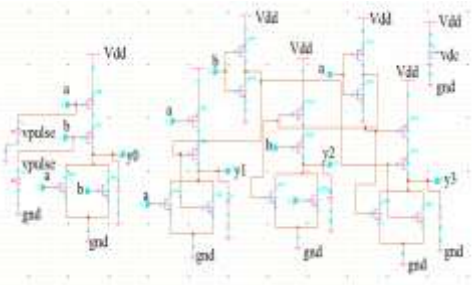

Figure 3: CMOS Proposed 2 inputs and 4 outputs Decoder in 90nm technology

It's Observed above figure 3 CMOS Proposed 2Inputs and 4Outputs Decoder in 90nm technology. CMOS Proposed 2Inputs and 4 Outputs Decoder simulation is completed in Cadence tool at 90nm technology. We proposed 2 inputs and 4 outputs decoder a and b are inputs then Outputs are like y0,y1,y2 and y3 equal to $yo = \overline{a}\,\overline{b}$, $y1 = \overline{a}b$, $y2 = a\overline{b}$ and $y3 = ab$ or $yo = \overline{a+b}$, $y1 = \overline{a+\overline{b}}$, $y2 = \overline{\overline{a}+b}$ and $y3 = \overline{\overline{a}+\overline{b}}$.

3.2 Switching activity

Switching activity is taken into account to be a crucial cause for dynamic power consumption additionally to voltage and physical capacitance (Veendrick 1984, Chandrakasan and Brodersen 1995). Although a chip will contain an enormous quantity of physical capacitance, there's no dynamic power consumption if not switched. The shift activity depends on information rate determines however typically on the average new data arrives at every node[17]. This information would possibly or may not show a discrepancy from the previous information worth. during this sense, the information rate f describes however typically on the average shift might occur. the information activity corresponds to the expected variety of transitions which will be triggered by the arrival of every new piece of knowledge. Thus it will be seen that f determines the common regularity of knowledge arrivals and α determines the amount of transitions that happens in every arrival[18].

3.3 Levels for Minimizing Power Consumption

The low power style involves the joint improvement of the parameters like voltage, physical capacitance and switch activity instead of freelance improvement (Najm 1994). a number of the precise power reduction techniques applicable at totally different levels of abstraction like technology level, circuit level and formula level ar mentioned during this section. Most of those techniques follow atiny low range of common themes as mercantilism area/performance for power, avoiding waste and exploiting neighborhood[19]-[20].

3.4 Circuit Level

Various circuit level techniques ar accustomed scale back the ability consumption like static, dynamic and pass semiconductor unit logic (Weste 1993). This is thanks to limited reproduction delays from one logic block to ensuing i.e., a node have multiple transitions in an exceedingly clock cycle previously subsiding to the right level. The capacity unwanted transitions could be perform of input patterns, private state assignments within the logic style, delay skew and logic depth. When it's attainable to ignore these transitions, dynamic logic doesn't have this inconvenience, considering any node will carry at the most one power overcoming transition per clock cycle[21]. In static CMOS circuits, it's found that there's an on the spot path from power offer to ground that cause tangency currents. Yet, filler transistors for equal tr (rise) and tf (fall times), the tangency part of the overall power is unbroken to but 2 hundredth of the dynamic switch part (Veendrick 1984). This drawback doesn't occur in dynamic logic, aside from those cases during which static pull up devices ar accustomed management charge sharing. the opposite circuit level style is Complementary Pass semiconductor unit Logic (CPL), that is one kind of logic that's standard in nMOS circuits (Weste and Eshraghian 1993, Yano et al 1990). The gate style uses solely nMOS transistors and needs the inverted input signals to implement Karnaugh maps for logic functions[22].

3.5 Threshold Voltage Reduction

One of the method parameters that encompasses a giant impact on circuit performance is threshold voltage (Chandrakasan et al 1992 and piano player et al 1994). the worth of the brink voltage is extraordinarily necessary at low supply voltages. the brink voltage places a limit on the minimum offer voltage which will be used while not acquisition unreasonable delay penalties. Based on this, it's going to be affordable to think about reducing threshold voltages in a low power method. Therefore, solely transistors that comprise delay essential paths ought to be changed and these circuits ar referred to as as multi- threshold circuits that attracted vital analysis interest (Wang and Vrudhula 2002, Wei dynasty et al 1999, Thompson et al 1997)[23].

IV. SIMULATION RESULTS

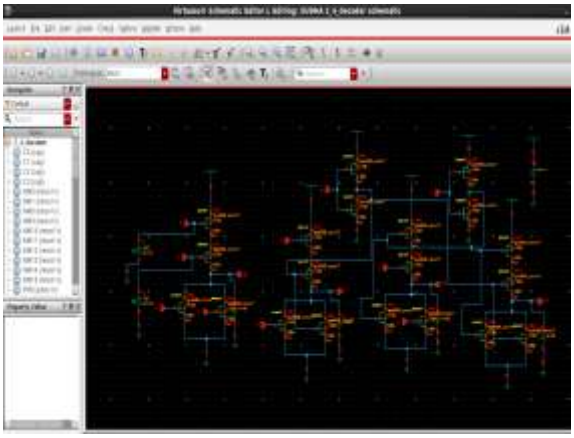

Figure 4: Proposed CMOS 2 inputs and 4 outputs Decoder in 90nm technology

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It is observed from the Figure 4, The PMOS and NMOS transistors schematic diagram consist of width are 240nm and 120nm at the frequency 10MHz and supply voltage 1 V. The simulation of the proposed CMOS 2inputs and 4outputs decoder schematic diagram was carried out using 90nm technology.

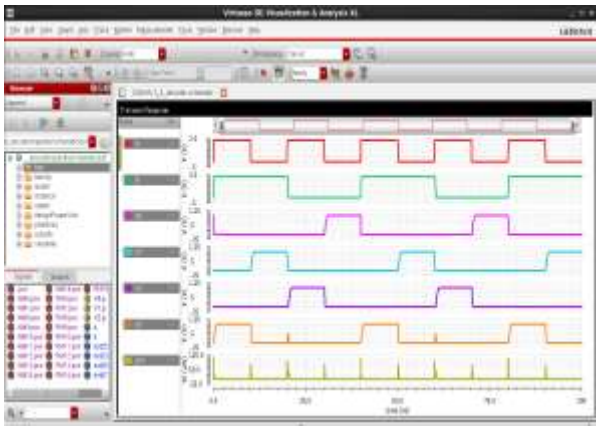

Figure 5: Proposed CMOS 2inputs and 4 outputs Decoder Output Waveform at 10MHz.

As shown in Figure 5 Proposed CMOS 2inputs and 4 outputs Decoder Output Waveform at 10MHz. Simulation result of output waveform at 1Volts at the frequency 10MHz in 90nm technology.

Table 2: Conditions

Conditions	PMOS	NMOS
Library name	gpdk90	gpdk90
Length	90nm	90nm
Total width	240nm	120nm
Figure width	240nm	120nm

Table 3: Simulation Results for Proposed CMOS 2 inputs and 4 outputs Decoder Power with 1 V supply in 90nm.

Capacitance(fF)	10,000	1,000	500	200	100	50	10
Dynamic power (µW)	68.56	23.74	20.68	16.56	10.34	5.438	1.399

It is observed from the Table 3. Proposed CMOS 2 inputs and 4 outputs Decoder, We have reduced Capacitance Sizing like (50fFand 10fF) 74% Dynamic Power Reduced using Cadence 90nm Technology.

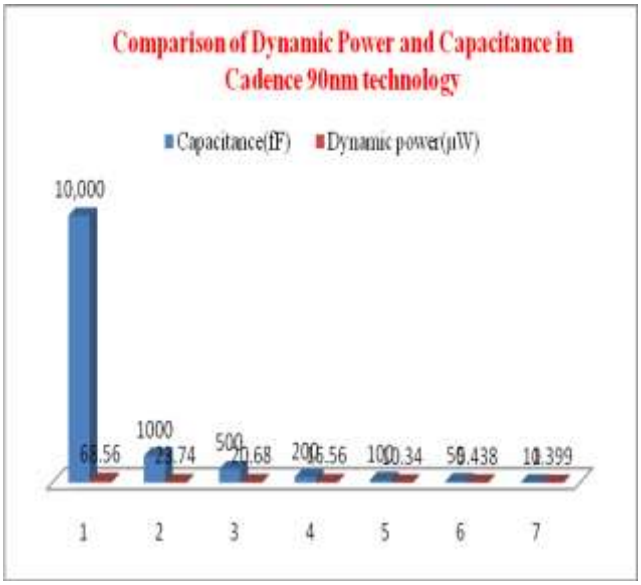

Figure 6: Comparison of Dynamic Power and Capacitance in Cadence 90nm technology

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It is observed from the Figure 6. Proposed CMOS 2 inputs and 4 outputs Decoder, We have reduced Capacitance Sizing like (10,000fF,1000fF,500fF,200fF,100fF,50fFand 10fF) Dynamic Power Reduced and Speed is increasing and Area Reduced using Cadence 90nm Technology.

Table 4: Simulation Results for Proposed CMOS 2 inputs and 4 outputs Decoder Delay with 1 V supply in 90nm Technology

Capacitance(fF)	10	50
Delay(nS)	21.01	23.65
Area(nm^2)	44.48	159.92

It is observed from the Table 3. Proposed CMOS 2 inputs and 4 outputs Decoder, We have reduced Capacitance Sizing like (50fFand 10fF) 11.16% Delay Reduced using Cadence 90nm Technology.

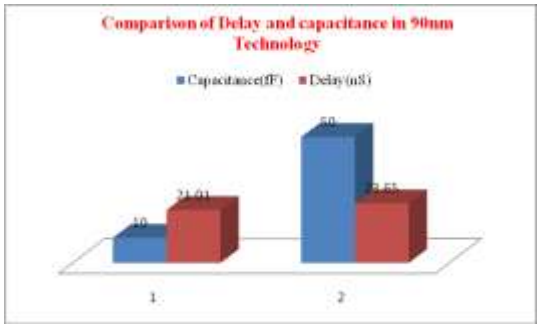

Figure 7: Comparison of Delay and capacitance in 90nm Technology

It is observed from the Figure 7. Proposed CMOS 2 inputs and 4 outputs Decoder, We have reduced Capacitance Sizing like (50fFand 10fF) Delay Reduced using Cadence 90nm Technology.

Table 5: Simulation Results for Proposed CMOS 2 inputs and 4 outputs Decoder Area with 1 V supply in 90nm Technology

Capacitance(f F)	10	50
Area(nm^2)	44.48	159.92

It is observed from the Table 5. Proposed CMOS 2 inputs and 4 outputs Decoder, We have reduced Capacitance Sizing like (50fFand 10fF) 74% Area Reduced using Cadence 90nm Technology.

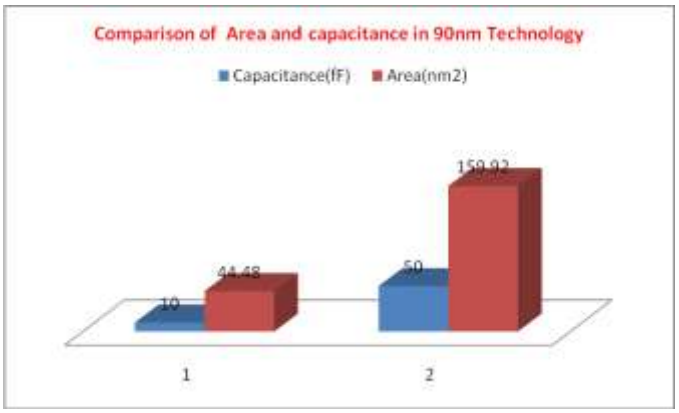

Figure 8: Comparison of Area and capacitance in 90nm Technology

It is observed from the Figure 8. Proposed CMOS 2 inputs and 4 outputs Decoder, We have reduced Capacitance Sizing like (50fFand 10fF) 72% Area Reduced in Cadence 90nm Technology.

V. CONCLUSION

The initial phases of analysis and development efforts in VLSI design were familiarized towards achieving high speed and miniaturization. At present, the growing trends in transportable computing and wireless applications demand the necessity to hunt out new technologies and style circuits that consume low power. This necessitates the necessity to orient the research towards reducing power dissipation in VLSI circuits. Recent trends within the growth and development of battery powered portable and mobile computing devices necessitate the necessity for extended battery life and thence lesser battery power consumption. The battery life is more reduced by the employment of high speed processors and huge recollections in them. Also, the magnitude of power dissipation per unit space within the integrated circuits of gift day microprocessors and recollections square measure chop-chop increasing due to the accumulated speed and flexibility. It is observed from the Table 3,Table4 and Table 5. Proposed CMOS 2 inputs and 4 outputs Decoder, We have compared capacitance sizing like (50fF and 10fF) in condition of power ,delay and area. We have reduced Capacitance Sizing like(50fF and 10fF), 74% Dynamic Power Reduced and 11% delay reduce and 74% Area Reduced in Cadence 90nm Technology.

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