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QCA Implementation of Ultra-Low Power High Speed Reversible 2×2 Array Multiplier

Vignesh M[1]
Assistant Professor[1]
Department of ECE
Hindusthan Institute of Technology
Coimbatore, Tamil Nadu, India - 641032
E-mail: vighcet08@gmail.com

Praveen G[2]
UG Scholar[2]
Department of ECE
Hindusthan Institute of Technology
Coimbatore, Tamil Nadu, India - 641032
E-mail: praveeng2565@gmail.com

SarathaPriya E[3]
UG Scholar[3]
Department of ECE
Hindusthan Institute of Technology
Coimbatore, Tamil Nadu, India - 641032
E-mail: sarathapriya22@gmail.com

Stephen Arul Doss P[4]
UG Scholar[4]
Department of ECE
Hindusthan Institute of Technology
Coimbatore, Tamil Nadu, India - 641032
E-mail: stephenarulp@gmail.com

Vijaya Kumar G[5]
UG Scholar[5]
Department of ECE
Hindusthan Institute of Technology
Coimbatore, Tamil Nadu, India - 641032
E-mail: vijaynaidug77@gmail.com

Abstract: Quantum-Dot Cellular Automata (QCA) is a developing nanotechnology that appears to be a good technology to replace the conventional Complementary Metal Oxide Semiconductor (CMOS) technology. This QCA has the advantages of very low power dissipation, faster switching speed and extremely low circuit area which can be used to design Nano Scale circuits. In this paper, the New Efficient QCA Designs of the basic Reversible Gates such as: CNOT gate, Feynman gate, Double Feynman gate are shown based on the straight interactions between the QCA cells. Also the designs of 4-bit Reversible Ripple Carry Adder and 2x2 Reversible Array Multiplier using the proposed efficient Reversible Gates are implemented. The proposed layouts are designed and simulated using QCA Designer Software. In comparison with existing Reversible Gate based QCA designs, the proposed layouts are implemented with the minimum number of cells, minimum delay and also minimum area without any wire-crossing techniques. Also, as compared to the CMOS technology, the proposed layouts are more efficient in terms of the area and power. Therefore, the proposed design can be used to realize quantum computation in Ultra-Low power circuits.

Keywords: QCA, CMOS, QCAD andReversible Gates.

I. INTRODUCTION

One of the most challenging problems in the development of computation paradigms and system is data loss. Reversible computation is a possible solution to solve this problem by allowing the computation to be done at the logical level without data loss by establishing a one-to-one mapping between the inputs and outputs of the circuit, that is, the number of inputs equal to the number of outputs.

Quantum-Dot Cellular Automata (QCA) is a promising emerging technology that works on novel paradigms such as synthesis of reversible gates[11]. QCA is a Nano electronic technology that gives another approach to computation at Nano level. Research and Development in the field of electronic devices during the last decades made it possible for the designers to decrease the size of the components and the power consumption. QCA is based upon the encoding of binary data in the electron charge configuration within quantum-dot cells. There is no current flow between cells and no outer source is delivered to singular internal cells due to the reordering of electron positions.

A cell is a Nano Scale device able to encode data by two electron configuration. The cells must be aligned exactly at Nano Scales to provide correct functionality; thus, the testing of the devices for misalignment and manufacturing errors has an important role for the correctness of circuits. The relation between computation and data loss has been resolved in QCA because it has very low power consumption that is a common property for QCA.

II. REVERSIBLE GATES

A. Feynman Gate(Controlled NOT Gate)

The Feynman Gate is a 2×2 Reversible Gate. Its two inputs *A* and *B* are mapped to the outputs *P* and Q as P=*A* and Q=A xorB[1]. The block diagram of the Feynman Gate is shown in Figure 1.

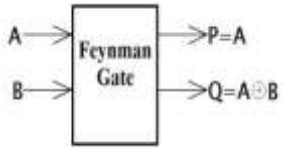

Figure1. Block Diagram Of Feynman Gate

The operation of Feynman Gate can be understood with the help of Table 1.

Table 1. Feynman Gate Truth table

Input			Output		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

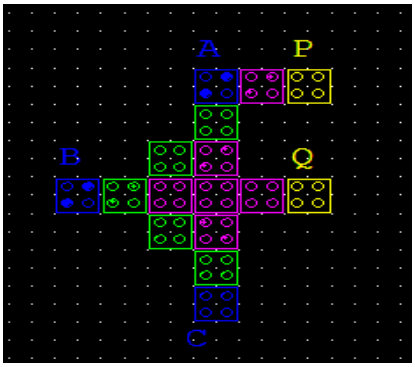

Figure 2.QCA Layout ofExisting Feynman Gate

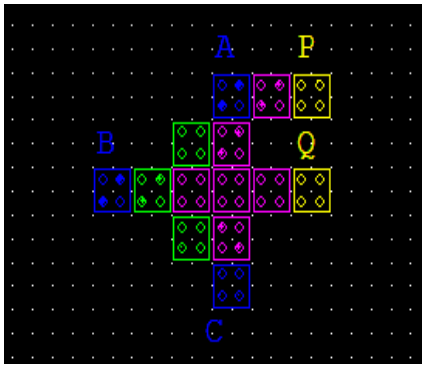

Figure3.QCA Layout ofProposed Feynman Gate

The QCA Layout Representations for the Existing & Proposed Feynman Gate are shown in Figure 2 and Figure 3.

B. Double Feynman Gate

This gate is also well known type of the basic reversiblegates having three numbers of inputs and three numbers ofoutputs. The inputs are denoted asA, B, C and outputs as P, Q, R and relationship can be givenas, P=A,Q=A xor B,R=A xorC[1]. The block diagram of the Double Feynman Gate is shown in Figure 4.

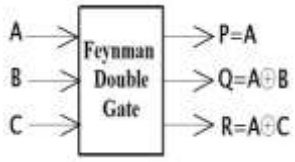

Figure4. Block Diagram of Double Feynman Gate

The operation of Double Feynman Gate can be understood with the help of Table 2.

Table 2. Double Feynman Gate Truth Table

Input			Output		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

The QCA Layout Representations for the Existing & Proposed Double Feynman Gate are shown in Figure5 and Figure6.

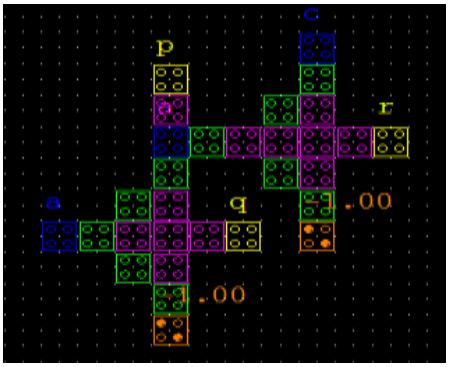

Figure5.QCA Layout ofExisting Double Feynman Gate

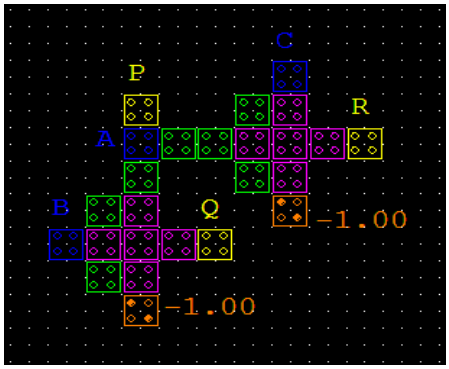

Figure6.QCA Layout ofProposed Double Feynman Gate

III. PROPOSED DESIGN

The proposed Reversible 2x2 Array Multiplier is designed in the following stages:

Stage 1: Design of Basic Reversible Gates
Stage 2: Design of Reversible Full Adder
Stage 3: Design of **4**-bit ReversibleRipple Carry Adder (RCA)
Stage 4: Design of Reversible 2x2 Array Multiplier

A. Design Layout of Basic Reversible Gates

The QCA designs of proposed Basic Reversible Gates are shown in the Section 2.

B. Design Layout of Proposed Reversible Full Adders

1. Feynman Gate based Full Adder

QCA Layout of Feynman Gate based Full Adder is shown in Figure7.

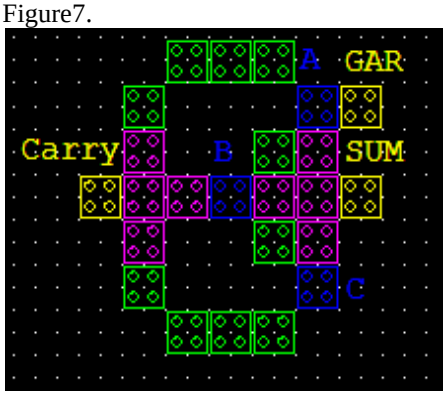

Figure7.QCA Layout ofFeynman Gate based Full Adder

2. Double Feynman Gate based Full Adder

QCA Layout of Double Feynman Gate based Full Adder is shown in Figure 8.

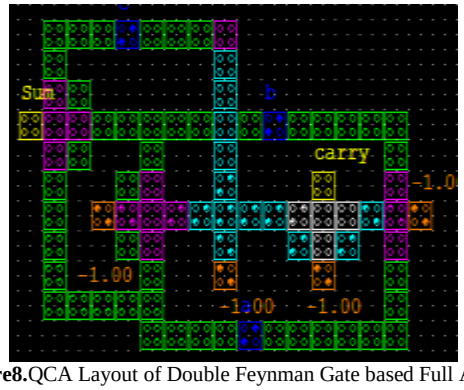

Figure8.QCA Layout of Double Feynman Gate based Full Adder

C. Design Layout of 4 bit Reversible Ripple Carry Adder

The 4-bit Ripple Carry Adder can be constructed by cascading the 4-Reversible Gate based Full Adders[8]. This section describes the designs of Feynman and Double Feynman Gate based Ripple Carry Adders.

1. Double Feynman Gate based Ripple Carry Adder

The QCA Layout of 4-bit Reversible Ripple Carry Adder isshown in Figure 9.

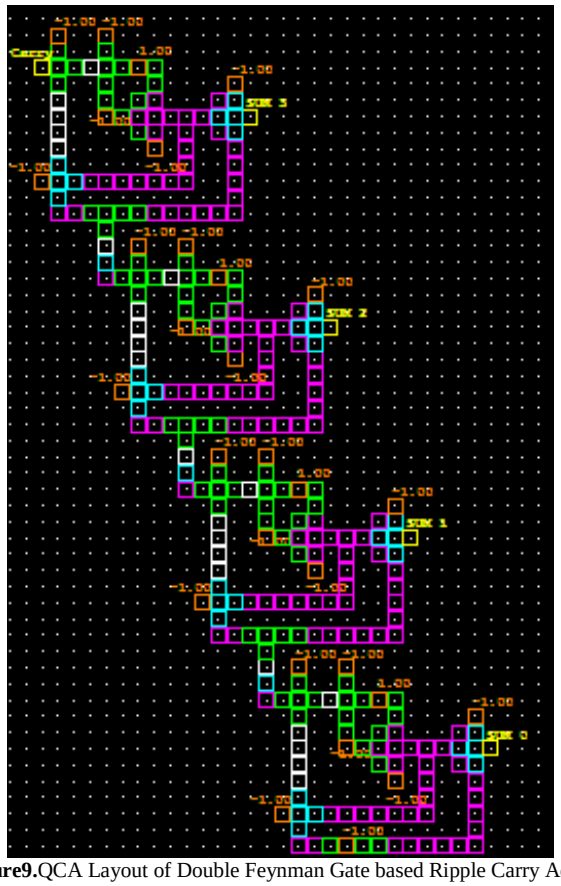

Figure9.QCA Layout of Double Feynman Gate based Ripple Carry Adder

2. Feynman Gate based Ripple Carry Adder

The QCA Layout of 4-bit Reversible Ripple Carry Adder is shown in Figure 10.

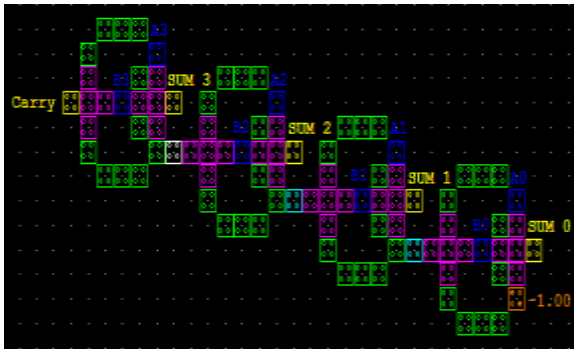

Figure 10.QCA Layout of Feynman Gate based Ripple Carry Adder

D. Design Layout of Reversible 2x2Array Multiplier

An array Multiplier is a digital combinational circuit that is used for the multiplication of two binary numbers by employing an array of full adders and half adders[3]. This array is used for the nearly simultaneous addition of the various product terms involved.

Here Feynman Gate based RCA is chosen for implementing the multiplier structure because of its improved delay and area when compared to the Double Feynman Gate based RCA. The QCA Layout of 2x2 Array Multiplier is shown in Figure 11.

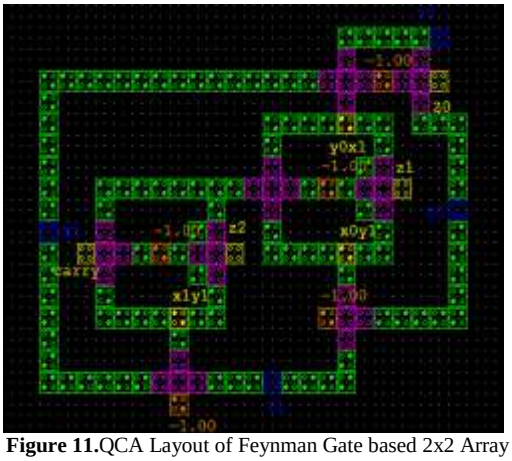

Figure 11.QCA Layout of Feynman Gate based 2x2 Array Multiplier

IV. RESULTS AND DISCUSSION

The proposed QCA layouts are simulated using QCA Designer Software version 2.0.3with the default parameters of the both Bistableand Coherence Vector Engines. QCA Designer Software is a powerful and fast tool can be used for the QCA layout design and simulation.

For both simulation engines the same results are achieved, which indicate the correctness of the proposed layouts.The results of bistable engine with the following parameters (default parameters) are used,

Number of samples	12800
Convergence tolerance	0.0001
Radius of Effect	65 nm
Relative Permittivity	12.9
Clock High	9.8×10^{-22} J
Clock Low	3.8×10^{-23} J
Clock Amplitude Factor	2
Layer Separation	11.5 nm

Maximum iteration per sample is 100 and randomized simulation order.Also, the QCA cells are assumed to have a width and height of 18 nm and their quantum dots have 5 nm diameter. As it can be seen that the proposed layouts work satisfactory and the outputs of all proposed QCA Reversible Gates generate thorough highly polarized signals, which can provide a high drivability for the QCA reversible circuits.

From the below comparison tables, it is clear that the proposed QCA designs has very less number of cells, area and delay when compared to the existing QCA designs.

A. Comparison Table for Basic Reversible Gates

The comparisons of parameters for the different reversible gates with the existing designs are shown in the Table 3.

Table 3. Comparison Table for Basic Reversible Gates

Designs	Area		Cell Count		Clock Cycle		Wire - Crossing
	Existing	Proposed	Existing	Proposed	Existing	Proposed	
Feynman Gate	0.02	0.01	16	13	3	2	No
Double Feynman Gate	0.04	0.04	30	24	4	2	No

B. Comparison Table for Adders

The comparisons of parameters for the different Reversible Gate based Adders with the existing designs are shown in the Table 4.

Table 4. Comparison Table for Adders

Designs	Area		Cell Count		Clock Cycle		Wire - Crossing
	Existing	Proposed	Existing	Proposed	Existing	Proposed	
Feynman Gate based FA	0.04	0.03	34	24	4	3	No
Double Feynman Gate based FA	0.11	0.09	100	89	4	3	No
Feynman Gate based 4-bit RCA	0.15	0.13	146	95	7	5	No

Double Feynman Gate based4-bit RCA	0.13	0.12	346	296	7	6	No

C. Comparison Table for Reversible 2x2 Array Multiplier

The comparison of parameters for the Proposed Reversible 2x2 Array Multiplier with the existing design is shown in the Table 5.

Table 5. Comparison Table for 2x2 Array Multiplier

Design	Area		Cell Count		Clock Cycle		Wire - Crossing
	Existing	Proposed	Existing	Proposed	Existing	Proposed	
Feynman Gate based 2x2 Reversible Array Multiplier	0.24	0.17	178	155	6	3	No

D. Simulation Output Waveform of the Proposed Array Multiplier

The Simulation Output Waveform of Feynman Gate based 2x2 Array Multiplier is shown in Figure 12.

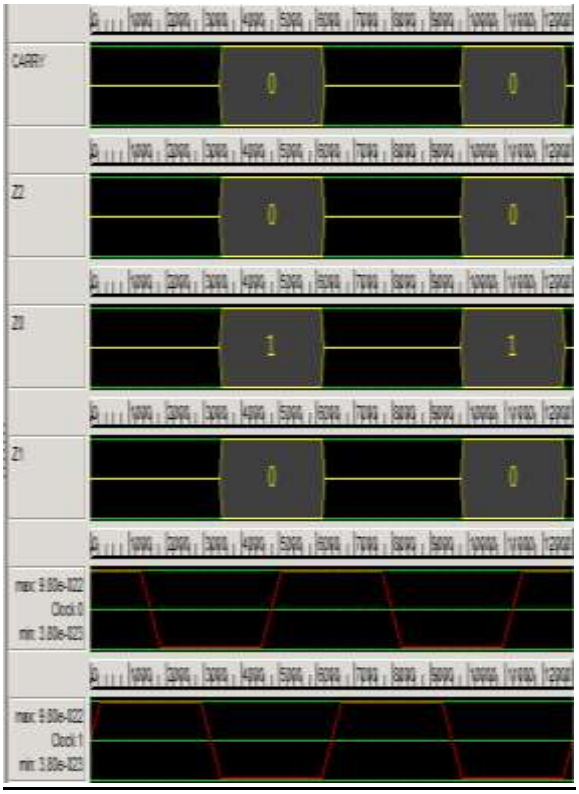

Figure12. Simulation Output Waveform of Feynman Gate based 2x2 Array Multiplier

V. CONCLUSION

In this project, we have designed New and Efficient QCA implementations of the basic Reversible Gates. Also, the efficient designs of Reversible Full Adders, 4-bit Reversible Ripple Carry Adder and Reversible 2x2 Array Multiplier are implemented using QCA. Our designs are able to overcome the drawbacks of the existing Reversible Gate based designs. The comparison table shows that the proposed reversible gate based designs are implemented with minimum clock cycles, cell count and area. Also our proposed QCA implementations are much denser in comparison with conventional CMOS implementations. The simulation results using QCA Designer software showed that our QCA implementations performed well. These new layouts can be simply used as suitable components for designing the High Speed and Ultra-Low Power consumption architectures in Nano scale reversible computing.

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AUTHOR'S BIOGRAPHIES

Mr. M.Vigneshis currently working as Assistant Professor in the Department of ECE at Hindusthan Institute of Technology, Coimbatore. He received his M.E Degree in VLSI Design from Info Institute of Engineering, Coimbatore and B.E degree in ECE from Hindusthan College of Engineering and Technology, Coimbatore. His research interest includes VLSI Design, Signal Processing and Image Processing. He has published 3 international journals and one national journal. He is a member of IETE and IACSIT. He has received Seminar Grant fund from CSIR. He has totally 4 years of teaching experience.

Mr. G.Praveen is an UG Scholar of ECE from Hindusthan Institute of Technology, Coimbatore. He is currently pursuing his Final Year B.E.

Ms. E.SarathaPriya is an UG Scholar of ECE from Hindusthan Institute of Technology, Coimbatore. She is currently pursuing her Final Year B.E.

Mr. P.Stephen Arul Doss is an UG Scholar of ECE from Hindusthan Institute of Technology, Coimbatore. He is currently pursuing his Final Year B.E.

Mr. G.Vijaya Kumar is an UG Scholar of ECE from Hindusthan Institute of Technology, Coimbatore. He is currently pursuing his Final Year B.E.