International Journal of Modern Electronics and Communication Engineering (IJMECE) ISSN: 2321-2152
Volume No.-7, Issue No.-2, March, 2019

Design and Analysis of Low-Voltage Low-Power Tri-state Buffers and its Application using 22-nm CMOS Technology

M. Madhusudhan Reddy1st
Dept. of Electronics and Communication Engineering
Jawaharlal Nehru Technological University Kakinada
Kakinada, India
E-mail: machupalliphd@gmail.com

M. Sailaja2nd
Dept. of Electronics and Communication Engineering
Jawaharlal Nehru Technological University Kakinada
Kakinada, India
E-mail: maruvada.sailaja@gmail.com

K. Babulu3rd
Dept. of Electronics and Communication Engineering
Jawaharlal Nehru Technological University Kakinada
Kakinada, India
E-mail: kapbbl@gmail.com

Abstract: In memory architecture, the standard Complementary Metal Oxide Semiconductor (CMOS) and clocked CMOS (C^2MOS) tri-state buffers lie in the critical path that affects the overall speed of the memory. The standard CMOS and C^2MOS logic based tri-state buffers require 12 and 8 Transistors. The internal circuitry in tri-state buffer is responsible for the huge time-delay and more power. Two novel tri-state buffer circuits have been proposed. They are Transmission Gate (TG) based tri-state buffer and pseudo-nMOS with active enable pull-up tri-state buffer, designed and examined using mentor graphics tool at 22-nm CMOS technology. The proposed tri-state buffer circuits are compared with existing ones by varying the supply voltage in the range of 0.4V-to-1V. The optimization of transistor count leads to the reduction of logical effort (G) and parasitic delay (p) of the circuit. The proposed TG tri-state buffer occupies less delay of about 47% and 31.8% when compare to existing ones for all considered supply voltages. The stacking effect contributes to reduced static power of about 36% and 33% using TG tri-state buffer as compared to CMOS and C^2MOS. The proposed TG tri-state buffer exhibits high speed and low power-delay-product (PDP) of about 72% and 66% as compared to existing ones. By using Euler's path approach, optimization of an area takes place by the TG logic based tri-state buffer by a factor of about 72.62% and 44.44% as compared to standard CMOS and C^2MOS tri-state buffers.

Keywords: Low-voltage Low-Power logic styles, Tri-state Buffers, D-Latch, Energy optimization, performance comparison.

I. INTRODUCTION

Mostly tri-state buffers are used to permit connectivity of the multiple signals on a single bus without any loss of information. These can be used internally in many integrated circuits and typically in processors, memories and peripherals. Generally tri-state buffers are classified into two types: active enable high tri-state buffer and active enable low tri-state buffer [1].

The explanation for the existing topologies for the tri-state buffer circuits is as follows,

1. The standard tri-state buffer consists of 1 NAND gate, 1 NOR gate and 2 NOT gates, when designed with respect to CMOS logic it needs 12 transistors. The main advantage of static CMOS logic is its robustness against to device variations, voltage scaling, easy to design, low-power and layout is straight forward with regular structure and supported by CAD tools to a great extent. But a major amount of delay and power is contributed by the tristate buffer. Because it requires more number of transistors to implement which occupies large chip area and higher operating speed is not possible due to large input capacitance [1] [2].

2. The conventional C^2MOS tri-state buffer consists of 6 MOSFET transistors designed with respect to C^2MOS logic. The advantages of dynamic C^2MOS logic over standard CMOS logic circuits are i. Occupies small area due to less number of transistors. ii. The parasitic capacitance of the circuit is small, so that higher operating speeds are possible. iii. The dynamic circuits operate under clock signal require careful clocking, consume more dynamic power. The circuit is sensitive to noise whenever the clock signal is operating in evaluation phase. Charge distribution is a major problem in the circuit design and must be considered [3] [4] [5].

In this paper, we presented two tri-state buffer circuits using TG logic and pseudo-nMOS with active enable pull-up logic. The proposed tri-state buffer circuits require less number of transistor counts and operate at higher speed with less energy consumption. The remaining part of the paper is organized as follows. Section 2 describes the design and analysis of tri-state buffer circuits. Section 3 explains the simulation results and performance comparison. An application (D-latch) is simulated using proposed tri-state buffers in section 4 and section 5 ended up with a conclusion.

II. PROPOSED TRI-STATE BUFFER CIRCUITS

A. *Transmission gate (TG) based Tri-state Buffer*

The tri-state buffer is designed with respect to TG logic requires 4 transistors as shown in Figure1. The parallel connection of two pass transistors i.e. M3 and M4 realize TG

logic provides a better driving capability. Here EN denotes the enable as active high input signal connected to the gate terminal of transistor M4 and its complement is connected to the gate terminal of M3 transistor. The signal A is the input connected to the source terminals of M3 and M4 transistors, drain terminals are shorted together and connected to the output. The operation of the proposed TG based tri-state buffer is shown in Table1. The TG logic requires lower transistor count as compared to CMOS and C^2MOS tri-state buffers which reduces the critical path delay and occupies less silicon area on the chip.

Table1. Functional table

EN	A	M1	M2	M3	M4	OUT
1	1	OFF	ON	ON	ON	1
1	0	OFF	ON	ON	ON	0
0	1	ON	OFF	OFF	OFF	Z
0	0	ON	OFF	OFF	OFF	Z

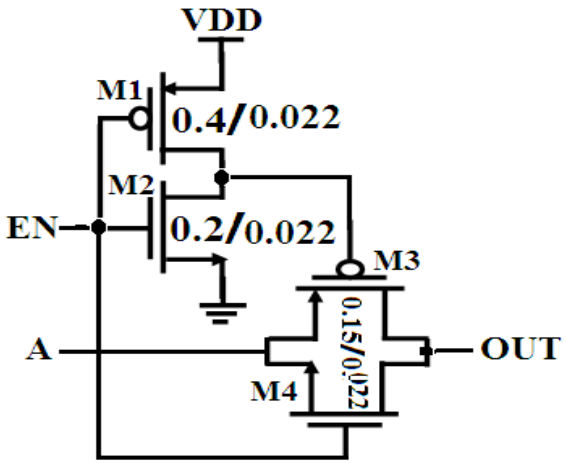


Figure1. Proposed tri-state buffer circuit using TG logic.

B. Pseudo-nMOS with active enable pull-up tri-state buffer

The tristate buffer is designed with respect to pseudo-nMOS logic with active enabled pull-up requires 5 transistors as shown in Figure2. The transistor M1 realize pseudo-nMOS logic, by connecting the gate terminal to the ground as shown in Figure2. The EN denotes enable as active high input signal connected to the gate terminal of M2 transistor and the input signal A is connected to the gate terminal of M3 transistor.

Table2. Functional table

EN	A	M1	M2	M3	M4	M5	OUT
1	1	ON	ON	ON	ON	OFF	1
1	0	ON	ON	OFF	OFF	ON	0
0	1	ON	OFF	ON	OFF	ON	Z
0	0	ON	OFF	OFF	OFF	ON	Z

The operation of the pseudo-nMOS based tri-state buffer is shown in Table2. It requires lower transistor count as compared to CMOS and C^2MOS tri-state buffer which reduces the critical path delay and occupies less silicon area on the chip.

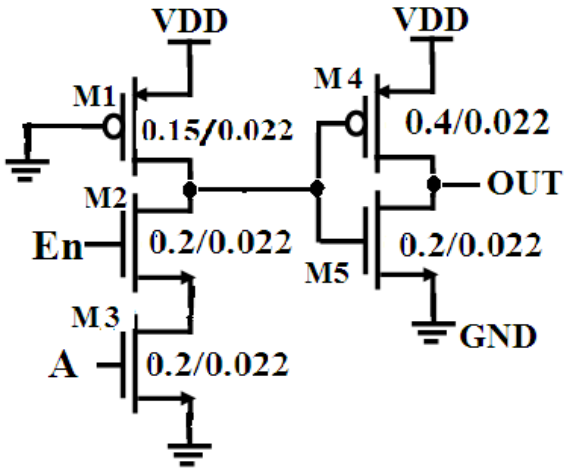


Figure2. Proposed tri-state buffer circuit using pseudo-nMOS logic.

III. SIMULATION RESULTS AND COMPARISONS

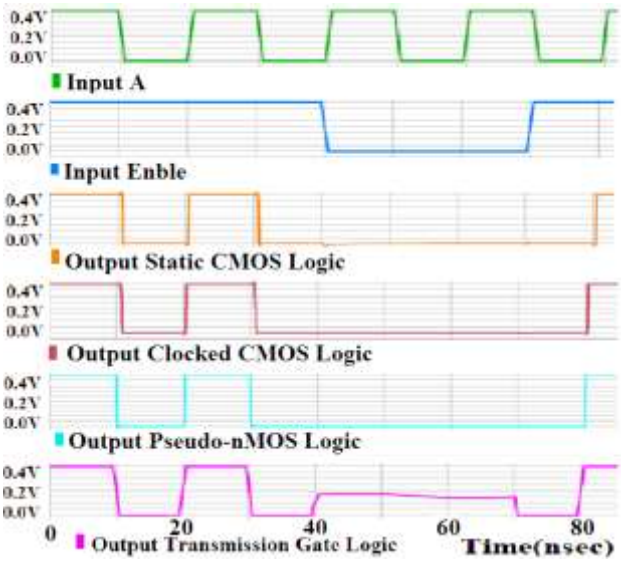


Figure3. Simulated waveform of the available and proposed tri-state buffers.

The proposed tristate buffer circuits are simulated using pyxis schematic of mentor graphics tool at 22-nm CMOS technology. The simulated waveforms of the existing and proposed tri-state buffer circuits are shown in Figure3. The proposed tri-state buffer circuits are compared with existing ones by varying the supply voltage in the range of 0.4-1V. The optimization of transistor count leads to the reduction of logical effort (G) and parasitic delay (p) of the circuit. The calculated theoretical values of G, P and minimum V_{DD} required for various tri-state buffer circuits is shown in Table3 [6].

The graph shown in Figure4 denotes the delay versus supply voltage. The proposed tristate buffer circuits occupy less delay for all considered supply voltages. The delay of the proposed tri-state buffer circuits is minimized due to optimization of the internal circuitry in tri-state buffer, responsible for the large

time-delay and huge power and reduced transistor count. The optimization of transistor count leads to the reduction of logical effort (G) and parasitic delay (p) of the circuit. The proposed TG tri-state buffer occupies less delay of about 47% and 31.8% when compare to existing ones for all considered supply voltages.

Table3. Comparison of design metrics for various tri-state buffers

tri-state buffers	logical effort (G)	parasitic delay (P)	transistor count	area (μm^2)	minimum V_{DD}
static CMOS	5.36	1.09	12	6.93	0.3
clocked CMOS	3.21	1.09	08	5.42	0.34
pseudo-nMOS	2.06	0.64	05	3.97	0.33
TG Logic	1.01	1.09	04	3.85	0.32

The graph shown in Figure5 denotes the dynamic power versus supply voltage. The proposed tri-state buffer circuits occupy less dynamic power for all considered supply voltages. The total capacitance i.e. C_{TOTAL} of the circuit depends on the input capacitance, switching, load capacitance (C_L). Due to reduced transistor count, minimization of capacitance takes place which is directly proportional to the dynamic power [6] as given by equation (1).

$$P_{Avg} = C_L V_{DD}^2 f \alpha \quad (1)$$

Where V_{DD} is supply voltage, C_L the load capacitance, f is the operating frequency. The proposed TG tri-state buffer exhibits high speed and low power-delay-product (PDP) of about 72% and 66% as compared to existing ones is shown in Figure6.

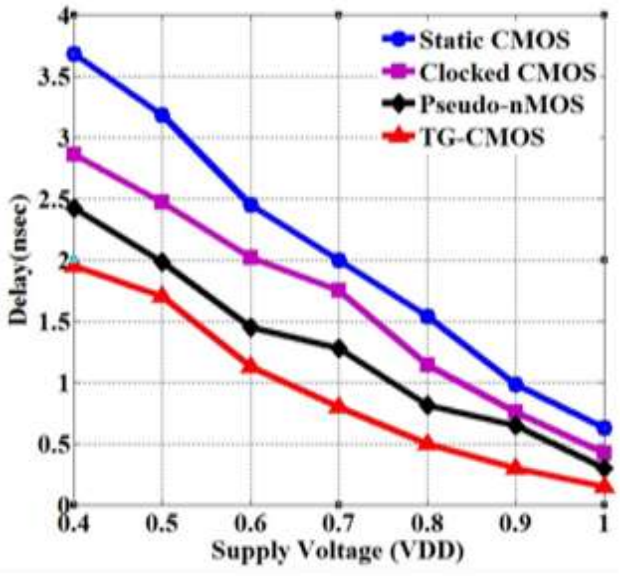


Figure4. Delay vs. Supply Voltage of different tri-state buffers.

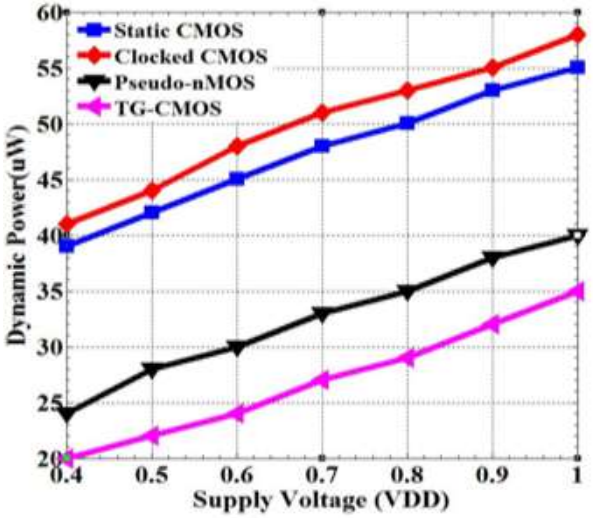


Figure5. Dynamic Power vs. Supply Voltage of different tri-state buffers.

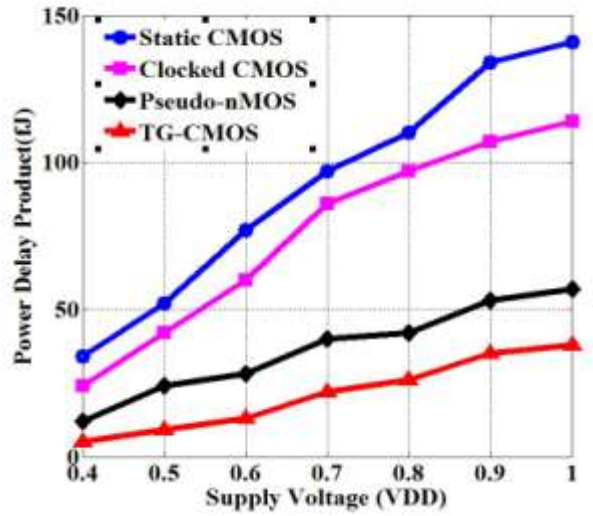


Figure6. Power delay product vs. supply voltage of various tri-state buffers.

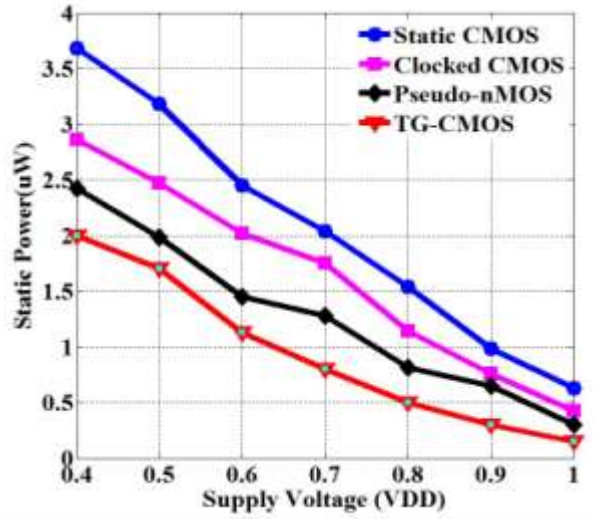


Figure7. Static Power vs. Supply Voltage of different tri-state buffers

The analytical model has shown that the transistors in stack should reduce the leakage current. i.e., if one transistor (I_{S1}),

two stacked transistors (I_{S2}), and three stacked transistors (I_{S3}) then it gives $I_{S3} < I_{S2} < I_{S1}$ respectively. If the number of transistors is more than three, then the leakage current becomes negligible. Hence the stack effect contributes to reduced static power reduction. The proposed design pseudo-nMOS with active enable pull-up tristate buffer gives more leakage power due to always ON transistor M1 but it can be reduced by the stacked transistors M1, M2 and M3. The TG based tri-state buffer gives less leakage power than all other logics as shown in Figure7 due to reduced transistor count. The stacking effect contributes to reduced static power of about 36% and 33% using TG tri-state buffer as compared to CMOS and C^2MOS [7].

A. Aspect ratios of the transistor

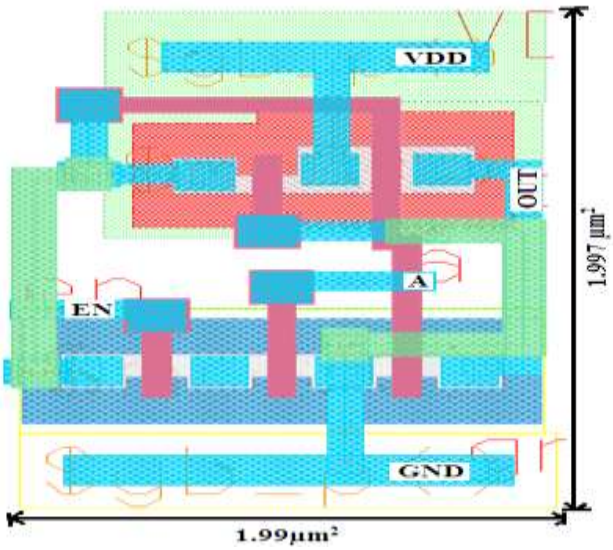
The power and delay of the circuit is inversely proportional to each other. In order to reduce the delay of the circuit, the aspect ratios of the transistor is increased by a factor of two which would increase the switching speed of the circuit. Increase of Width-to-Length ratios will increase the gate capacitance, load capacitance and area of the circuit leads to dynamic power dissipation [7]. To keep the tri-state inverter area within the reasonable value and to attain better performance of the tri-state inverter circuit, maintain the sizes of all the transistors for the proposed tri-state inverters and standard tri-state inverters are given by

$$\left(W/L\right)_{pMOS} = 0.4\mu m / 0.022\mu m$$

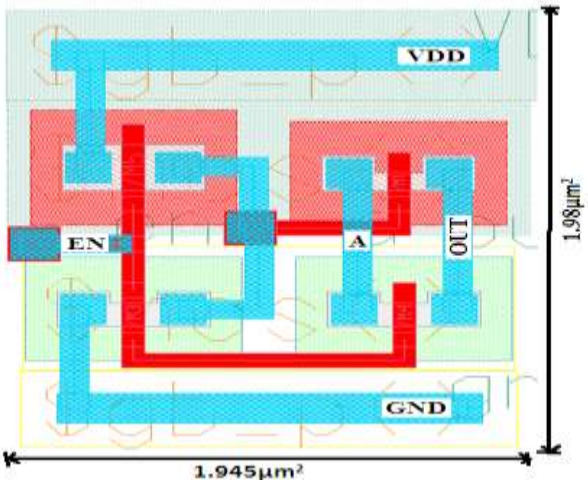
$$\left(W/L\right)_{nMOS} = 0.2\mu m / 0.022\mu m$$

For this purpose BSIM3 LEVEL 53 nMOS. 1 model and pMOS. 1 model transistors with V_{Tn} = 0.2 V and V_{Tp} = -0.2 V are used.

B. Comparison of area



(a)



(b)

Figure8. Proposed tri-state buffer layout using (a) Pseudo-nMOS with active enable pull-up (b) TG logic.

The layout of the proposed tri-state buffer structures is shown in Figure8 using mentor graphics IC layout 0.13 µm CMOS technology design rules. Because of the space constraint the layout of the other tri-state buffers are not shown. But the numerical value of the area occupied by the tri-state buffer circuits is shown in Table3. By using Euler's path approach [8], optimization of an area takes place by the proposed TG logic based tri-state buffer by a factor of about 72.62% and 44.44% as compared to standard CMOS and C^2MOS tri-state buffers. When compare to standard CMOS and C^2MOS tri-state inverters, the proposed ones occupy less amount of silicon area on the chip due to reduced transistor count.

IV. IMPLEMENTATION OF D-LATCH USING TRI-STATE BUFFER CIRCUITS

In the architecture of memories, a tri-state buffer plays an important role in read/write operations of the memory cell in the array. The circuit diagram of D-Latch using two tristate buffers with active high enable is shown in Figure10. The operation of the circuit is as follows: when the clock pulse is high, the buffer B1 is transparent and B2 is in high-impedance state, hence input D is present at the output Q. When the clock pulse is low the buffer B1 is in high-impedance state and B2 is in normal state, hence the loop preserves the previous state.

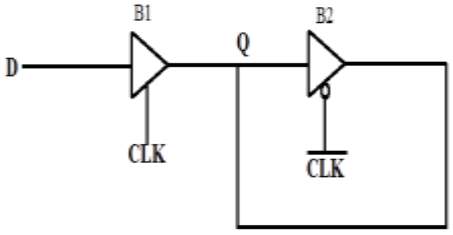


Figure9. Circuit diagram of a D-Latch.

The performance (design metrics) of the D-latch using different tri-state buffers are shown in Table4. The implementation of D-latch using proposed tri-state buffer structures having better delay performance and less energy consumption due to reduced critical path and transistor count.

Table4. Comparison of design metrics for D-Latch circuit

D-Latch	logical effort (G)	parasitic delay (P)	transistor count	area (μm^2)	minimum V_{DD}	Static power (µW)	Delay (nsec)	Dynamic Power (µW)	PDP (fJ)
static CMOS	36.3	4.39	24	11.3	0.50	7.30	9.90	60.92	603.1
clocked CMOS	21.2	4.39	16	9.84	0.58	5.37	5.81	45.35	263.4
pseudo-nMOS	15.1	3.42	12	8.56	0.52	3.62	4.28	30.68	131.3
TG Logic	11.3	4.11	08	6.95	0.50	2.83	3.40	28.81	97.95

V. CONCLUSION

This paper presents two tri-state buffer circuits using TG logic and pseudo-nMOS with active enable pull-up logic. The critical path produced due to the internal circuitry of the tri-state buffer reduces both the size and count of the transistors. With this, the logical effort, parasitic delay and C_{TOTAL} of the tri-state buffers are minimized, which exhibits better delay and energy performance. The proposed tri-state buffer circuits are compared with existing ones by varying the supply voltage in the range of 0.4V-to-1V. The proposed TG tri-state buffer exhibits high speed and low power-delay-product (PDP) of about 72% and 66% as compared to CMOS and Clocked CMOS circuits. An optimization of an area takes place using Euler's path approach by the TG logic based tri-state buffer by a factor of about 72.62% and 44.44% as compared to standard CMOS and C^2MOS tri-state buffers. For high performance, low-power and high-density memory architectures used in mobile and storage applications, the essential benefits of the proposed tri-state buffers could be fully utilized.

ACKNOWLEDGMENT

The authors wish to the higher authorities of Jawaharlal Nehru Technological University Kakinada, Kakinada for providing Research and Development lab to carry out research work.

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AUTHOR'S BIOGRAPHIES

M. Madhusudhan Reddy was born in Deganavandla Palli, Y.S.R district, Kadapa, (A.P), India in 1988, received the B.Tech degree in electronics and communication engineering from Sri Venkateswara University, Tirupathi in 2009 and Master of Technology in VLSI Design from Vignan's University, Guntur, India in 2012. Currently pursuing Ph.D. in the area of research is low-power VLSI design at Jawaharlal Nehru Technological University Kakinada, East Godavari, India.

Dr M. Sailaja was born in East Godavari, (A.P), India, in 1966, received the B.Tech degree in electronics and communication engineering from Sri Venkateswara University, Tirupathi in 1987, M.S from North Carolina state university, the USA in 1992 and Doctoral Degree in the field of ATM Networks from JNT University, Hyderabad in 2009. Currently working as a professor in ECE department, JNTUK, Kakinada, A.P, India. She has 23 years of

teaching experience and 12 years of research experience. Areas of interest are Microprocessors & Microcontrollers, Computer Organization and Low-power VLSI Design and published 30 research papers in reputed national and international Journals. Dr. M. Sailaja is a member of professional bodies such as M.I.S.T.E., M.I.E, IETE (Fellow).

Dr K. Babulu was born in East Godavari, (A.P), India, in 1971, received the B.Tech degree in electronics and communication engineering from Andhra University, Vishakhapatnam in 1993, Master Degree from REC Warangal, Andhra Pradesh in 1997 and Doctoral Degree in the field of VLSI & Embedded Systems from JNT University, Anantapur in 2010. Currently working as a professor in ECE department, JNTUK, Kakinada, A.P, India. He has 20 years of teaching experience, 2 years of industrial experience and 10 years of research experience. His areas of interest are Low-power VLSI Design, Embedded systems & Signal Processing and published 40 research papers in reputed national and international Journals. Dr. K. Babulu is a member of professional bodies such as IEEE (Senior Member), ISTE (Life Member), IE (Fellow) and IETE (Fellow).