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High Speed Multi-Rate Decimation Filter with Optimized Area for Efficient FPGA design

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Abstract: In this paper aspeed and area efficient decimation filter is proposed for high performance FPGA implementation for wideband converters. The design is optimized for area and suited particularly for filters with high decimation factor. The filter offers a decimation factor of 128 having input from Sigma-Delta Modulator. For achieving high speed operation of Decimation filter We have employed efficient design procedures in the form of pipeline architectures, polyphase decomposition, retiming structures, Canonical Sign Digit encoders and resource sharing. These techniques have been used for designing the optimally selected multi stage filers like Non-Recursive Comb filters, Cascaded Integrated Comb Filters and Half Band Filters. Each filtering stage is placed before or after another filter while keeping all the speed, area and power consideration up to an efficient level. The filter offers reduced word-lengths effects thereby providing increased speed and reduced power consumption. From the results it is shown that a better power conservation is achieved along with minimum consumed area while achieving high speed performance in the form of less design complexity. Experimental results show that the proposed filter design can prove one of the best options for future design consideration of decimation filter for Sigma Delta Analog to Digital converters.

Keywords: Decimation Filter, Comb Filter, Polyphase Decomposition, Canonical Sign Digit (CSD), Oversampling, Sigma Delta Converter.

I. INTRODUCTION

With the need of hand-held and portable personal communication systems growing day by day the design of small size, low power, secure and high performance devices is also growing [1, 2, 3]. Therefore, it is required to have an efficient, reliable and flexible signal processing. Moreover, due to the fast progress and rapid scaling of CMOS technology, digital signal processing (DSP) systems have almost replaced analog ones.

Analog to digital converter (ADC) forms an important section of a signal processing system and it may be a continuous or a discrete type. Currently an efficient choice for data converters is an oversampling ADC due to its small silicon area, low power consumption and higher resolution unlike traditional ones having Nyquist frequency limit [4]. The oversampling ADCs sample analog signal with higher sampling rate than Nyquist rate, which is usually expressed through oversampling ratio (OSR). Also, particularly they are favored for high speed applications as they are relatively simple and possess resistance against component mismatch and circuit errors.

Compared to traditional data converters, perhaps one of most important advantage among various others is their ease of implementation on a high-speed single chip VLSI circuit. Broad understanding of data converters can be obtained in [5, 6]and references therein.Presently ΣΔ ADCs are the best converters used for implementation in nm CMOS technology. The applications of ΣΔ ADCs are increasing day by day in different areas like wideband applications (SDR, LTE etc), medical and audio applications. Several papers that deal with different implementation architectures of decimation filter architecture in case of ΣΔ ADCs are available in literature.

As FIR filters are extremely stable and possess linear phase characteristics they are widely used in DSP applications [7, 8]. Therefore, in the research community significant attention has been given to the optimized implementation of finite impulse response (FIR) filters in hardware. Also there exist several issues while designing and implementing a digital filter like area, power consumption, and magnitude and frequency response.

Usually power consumption in a circuit is reduced by decreasing either of operating voltage or clock rate. But in case of ΣΔ ADCs the power consumption will increase as it utilizes oversampling at high clock rates. Also circuit delay increases on lowering the operating voltage which clearly will put a limit on operating frequency. Different solutions were proposed from time to time among which one is parallel processing. Traditionally, in signal processing parallel structures have been implemented by polyphase decomposition [9].

As such DSP functions are usually implemented on dedicated DSP processors or Application Specific Integrated Circuit (ASICs). While as DSP processors are flexible and less expensive but offer low speed for operation, ASICs have high speed but have cost and flexibility problem. So an alternative approach is provided in the form of Field Programmable Gate Arrays (FPGAs) as such they offer all above advantages and remove problems. Also as FPGA architectures offer

systemprogrammability the functionality of the device can be modified as per the need.

Several papers have proposed methods to reduce power consumption but at the expense of increased area [10-14]. Others have used only recursive filter algorithms at initial stages of decimation filter [15-18]. This work seeks to better the factors that like power consumption speed of operation along with the minimum possible area utilization while implementing complete decimation filter. The use of HBF's and conventional FIR filters ensure that stopband and passband response did not get affected. In this paper we discuss the design and implementation of low power high speed decimation filter using non-recursive as well as recursive filter algorithms and the designs are compared.

Keeping in mind that there have been several factors reported that effect the performance of a multistage filter design, there is need to keep them in a range desirable for an optimal design. Fr example, it has been shown that the total number of stages and their rate changing factors have considerable effect on filter latency and area while as memory usage, computational cost and their realization methods affect the power consumption [19]. So there is a demandable research work needed to design a model that considers the mentioned aspects for optimal multistage design.

The starting point in this work is the ΣΔ modulator and decimation filter specification. According to these specifications model of ΣΔ modulator is designed in the Matlab with the techniques fulfilling these specifications. The Matlab model and the architecture are designed and modified simultaneously if needed, to meet the correct functionality. The filter model created in Matlab is then translated into HDL code required for implementation of the design. The filter is then implemented in using this code in the Xilinx platform. Finally, this HDL model is synthesized successfully in Xilinx.

II. DECIMATION FILTER ARCHITECTURE

A decimator is a down-sampling filter whose function is to decrease the frequency of the output from the oversampled modulator up to the Nyquist rate. Another function of the decimation filter is to keep the passband aliasing within the prescribed limits.In sigma delta modulator (ΣΔM), the signal is oversampled and quantization error is shaped and pushed to higher frequencies of stop band. Therefore, outside signal band most of the power of quantization noise is present which can be easily filtered out by a digital filter following ΣΔM. The modulator includes of a loop filter (integrator) in forward path i.e. H (s), single or multi-bit quantizer, and a DAC in feedback path. The decimator includes a decimation filter followed by a down sampler.

In this scenario, the function of the decimator is to decrease the frequency of the output from the oversampled modulator up to the Nyquist rate. Decimation is performed by an integer factor by removing the samples from a sequence until the required sampling rate is obtained. Another function of the decimation filter is to keep the passband aliasing within the prescribed limits. Usually the input signal to the decimator is band limited in order to avoid aliasing after decimation. This is done by a low pass anti-aliasing filter before the removing of samples.

There are several architectural options available for implementing a decimation filter:

A. Comb Filter

One of the most important breakthroughs in the decimation filter design was achieved by E. Hogenaeur who put forward decimation filter which is highly area efficient. The filter presented reduced complexity and storage issues that were usually present with conventional FIR filters. These filters require no multipliers, which are responsible for area increase in a silicon chip. Also they use limited storage of coefficients as usually only additions/subtractions are required. These filters are designated as cascaded-integrated-comb (CIC) filters after their architectural configuration as they consist of combs (differentiators) and integrators.

Sinc filters are conventionally use CIC filters for the implementation.CIC filters can be used to implement multistage decimation filters economically. The transfer function of a CIC filter is:

$$F(z) = F_I^k(z) F_c^k(z) = \left(\frac{1-z^{-DN}}{1-z^{-1}}\right)^k \qquad (1)$$

Where F_I is the transfer function of the integrator part of the filter, F_C is the transfer function of the comb part of the filter, k is the order of the filter, i.e. number of sections of the comb part or the integrator part as they are equal, N is the decimation factor and D is differential delay where D = 1 or 2.

Implementation of transfer function of decimation filter results in the architecture as shown by block diagram in Fig. 3.

Hogenauer's[20] CIC filter structure also called IIR-FIR structure comprise of an equal number of integrator (IIR) and comb (FIR) filter stages. Also due to the presence of the IIR section they are also called recursive filters. The frequency response CIC filter can be easily tuned by simply selecting the appropriate number of integrator and comb filter pairs. It provides a designer with a hardware efficient implementation due to its highly symmetric structure.The CIC filter is an area-efficient, symmetric FIR filter having phase linearity.

The block diagram of CIC filter is shown in Fig. 1. Here in the circuit, the IIR filters work at F_s and the FIR filter works at Nyquist rate (F_N). Due to this configuration power consumption

of this filter is reduced significantly. Furthermore, area reduction is achieved due to absence of multipliers and comparatively less number of registers and adders.

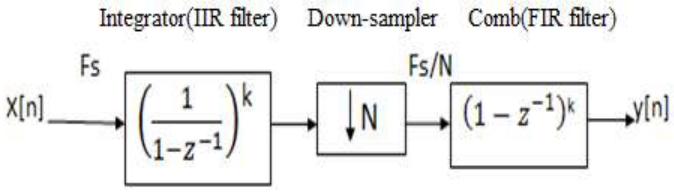

Figure 1. Block diagram of Comb decimator

The block supports real and complex fixed-point inputs. In its normal mode of operation, the CIC Decimation block allows the adder's numeric values to overflow and wrap around. The Fixed-Point infrastructure then causes overflow warnings to appear on the command line. This overflow is of no consequence. As the whole circuit is working at input sampling frequency which is very high, the power consumption of the circuit will be high. So a different decimation filter architecture is required in order to reduce power consumption. Other architectural options are the efficient non-recursive and polyphase structures; half band filters (HBFs) and several other modified structures. Register overflow can be avoided by setting the word length of the IIR filter equal to w + k. $\log_2$N, where w is the length of the modulator output [20].

B. Non-recursive filters

A modified transfer function can be obtained from original comb decimation filter one by simplifying Eq. (1) [22]to:

$$H(z) = \prod_{i=0}^{M-1}\left(1 - z^{-2i}\right)^{k} \qquad (2)$$

Where decimation factor N = 2^M. An effective way to realize this decimation filter is by using a cascade of $\log_2$N FIR filters each providing a decimation factor of 2. This is called 'non-recursive structure' because recursive IIR is not present in the architecture and is wholly realized by only FIR filters unlike IIR-FIR structure which is recursive one due to presence of IIR filters. Thus stability related issues are absent in this structure. Fig. 2, shows block diagram of non-recursive decimation filter.

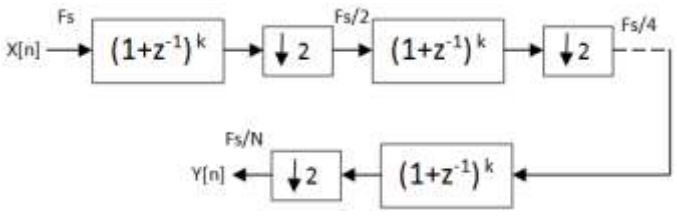

Figure 2. Non-recursive decimation filter structure.

Where x[n] is the output from ΣΔ modulator whose word-length is 'b' bits. The word-length increases by 'k' bits through each stage while the sampling rate decreases by a factor of 2 starting from Fs. The reduction of sampling rate in the earlier stages results in reduction of the power consumption.

C. Polyphase Decomposition

A limitation of the decimation structures discussed previously is that at the higher sample rate digital filtering is performed which results in effects like higher power consumption. The
limitation can be avoided by using a technique called polyphase decomposition of the filters [7]. An *N*-component polyphase decomposition of a digital filter can be performed such that the transfer function of the filter can be rewritten as:

$$H(z) = \sum_{i=0}^{N-1} z^{-i} E_i(z^M) \qquad (3)$$

Where $E_i(z)$ are the polyphase components of the filter $H(z)$. For the case when $M = 2$ we obtain

$$H(z) = E_o(z^2) + z^{-1} E_1(z^2) \qquad (4)$$

Using polyphase decomposition technique all filtering can be done at the lower sampling rate which will improve the efficiency of an implementation significantly with respect to power consumption [21].

Polyphase decomposition used for decimation is illustrated in Fig. 3.

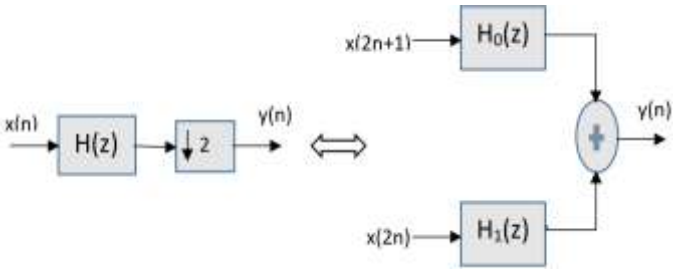

Figure3. Polyphase decomposition conversion

For multi-rate signal processing applications one of fundamental structure is the polyphase decomposition [22]. The reason is that it forms an efficient implementation of decimation filters due to reduction in the computational complexity by decimation factor, N. Another important advantage is parallel processing realization. Polyphase structure is usually modeled by employing commutator mode scheme [7]. One of the biggest advantages of polyphase decomposition is that it reduces the sampling frequency of comb based decimation filter which results in reduced power consumption.
As output of comb is decimated by factor 2 in case of non-recursive structure, half of the output is wasted. This results in increased power consumption and wastage of computational resources. If polyphase decomposition is used, we can get an improved structure and a more efficient implementation. The transfer function of each non recursive filter stage is given as:

$$E(z) = (1 + z^{-1})^{k} = E_0(z^2) + z^{-1}.E_1(z^2) \qquad (5)$$

Let us take an example where k=3. Thus

$$E(z) = (1 + z^{-1})^3 = 1 + 3z^{-1} + 3z^{-2} + z^{-3}$$
$$= 1 + 3z^{-1} + z^{-1}(3 + z^{-2}) \qquad (6)$$

Let us take $H_0(z)$, $H_1(z)$ as

$$E_0(z) = (1 + 3z^{-1}) \quad (7)$$
$$E_1(z) = (3 + z^{-2}) \quad (8)$$

This is implemented in Fig. 4.

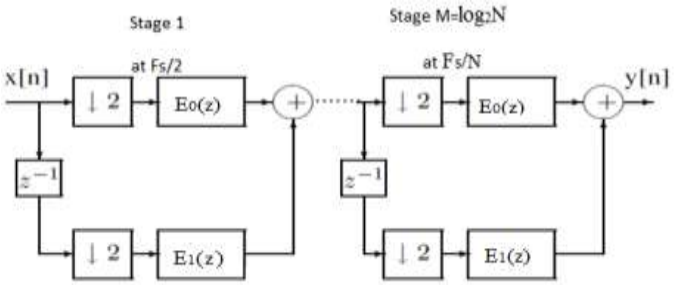

Figure4. Block diagram of a non-recursive polyphase decimation filter.

The sub-filters $E_0(z)$ and $E_1(z)$ can be implemented by different approaches which may or may not be multiplier free [23]. Similar to decimation factor of 2 other decimations can be obtained which are simply multiples of two.

a. POLYPHASE IMPLEMENTATION SCHEME:

Implementation of polyphase FIR filters is usually done either in transposed form (TF) or direct-form (DF) **[7]**. Although adders in both of these structures are same in number, delays in TF are lesser. But these delays in TF have larger width. Furthermore, the critical path in case of TF FIR filter consists of only a single multi-operand adder and single multiplier while DF has [N/M] multi-operand adders and one multiplier, where M and N are the decimation factor and filter order, respectively. Moreover, TF has multiplier optimization procedure due to its multiplier sharing structure.

In [21] DF has been chosen for implementation. Current architectures use polyphase decomposition because it results in operating frequency reduction such that critical path no longer remains an issue. For optimization many others in literature have utilized the TF to take advantage multiplier sharing. Hybrid structures have also been chosen some authors in which combination both the TF and DF structures is employed for designing a decimation filter.

b. POLYPHASE SPEED IMPROVEMENT METHOD

There are several methods in literature for increasing the speed of operation of CIC filters more and more. One such technique is proposed in [**16]**, where parallel CIC pre-filters are used which combine the qualities of CIC and polyphase decomposition. These filters help to achieve a large amount of hardware saving (particularly when decimation factor is high), and large speed increase in digital decimation filters. This speed improvement is achieved by achieving many times higher clock rate by paralleling computations. The proposed method reduces the area complexity of polyphase decomposition because resulting filter does not have multipliers. The increase in speed is clearly due to the use of polyphase decomposition approach.

D. Canonical Signed Digit Technique

For cost efficient implementation shift-and-add operations of constant multiplier can be used. This allows the designer to reduce the arithmetic complexity of the shift-and-add multiplier through several techniques. One of the most efficient techniques is the use of canonic signed-digit (CSD) code for representation of the coefficients [3]. CSD method, a cost reduction representation, is used to represent a signed number with the least possible number of non-zero digits, such that number of multiplications is reduced. CSD representation of coefficients has three digits set {-1, 0, 1}. This representation allows a coefficient implementation requirement to fewer adders/subtractors which results in a faster more compact multiplier.

III. PROPOSED DECIMATION FILTER

In this paper we design a decimation filter for 0.7-10 MHz range and is targeted for wideband SD ADCs used in state of art communication modules. The proposed filter is a high speed, low power and area optimized filter with down-sampling ratio of 128. However, the decimation rate can be easily programmed as per need of application by simplyselecting different sampling rates according to bandwidth of input signal. The proposed filter comprises of a recursive comb (CIC), two non-recursive comb, two HBFs and one FIR filter. In each filter the polyphase architecture is also used for implementation in order to minimize the increase the speed of operation and reduce power consumption. The use of FIR filters in the proposed design is due to the advantages highlighted in Table 1.

Table 1: Comparison of FIR and IIR filters

FIR	IIR
Always stable	Critically stable
Linear phase response	Non-linear phase response
Low sensitivity to quantization effects	Poor quantization properties
Preferred for sample rate conversion	Merely used for sample rate conversion
Simple extensions to multi-rate filters	Not preferred usually
High order filters require to do the job	Efficient low order filters
Computationally complex	No complexity issues
Transient response is longer	Shorter transient response

The first stage of proposed filter is a decimation by 2 non-recursive filter and second stage is a decimation by 4 CIC filter stage. The advantage of multistage design is that one can operate most of the filter architecture at a lower clock frequency compared to single stagethereby reducing the hardware complexity. After the first two stateswe employ Half Band Filter (HBF) as the third filtering stage with decimation factor of 2. The HBFensures a nice passband to stop band transition. A fourth type of filtering stage in the form of FIR filter is usedensure the droop compensation introduced by the initial stages and hence acts as equalizer at the end. The Table 2 describes the configuration of various filtering used in this work.

Table 2. Configuration of filters used in the proposed architecture

Stage	Type	Order
1st	Non-recursive comb Filter	4th
2nd	Non-recursive comb Filter	3rd
3rd	CIC Filter	3rd
4th	Half Band Filter	6th
5th	Half Band Filter	14th
6th	FIR Filter	36th

In order to achieve efficient performance and best optimization various techniques are employedtodesign the proposed decimation filter. The employed techniques are: Pipelining, Multi-rate filtering,Resource sharing, Retiming [25]. Also we haveemployed power efficient number systems like Canonical Signed Digits (CSD). Also, in order to achievethe linear phase response,all the filtersare designed with symmetric impulse response.

A. 1st and 2nd stage of Filter

As mentioned earlier, the first and second stage of the proposed decimation filter design are non-recursive. However, the first stage is of fourth order and 2ndstage is of third order. The advantage higher speed and low power consumption offered by the non-recursive filters ensures the highcircuit speed [26] (Bibin John). It has been shown that for a nth-order modulator the order of the anti-alias filter should be one up in order for meeting the anti-aliasing requirements [24].As described earlier that for the 3rd order modulator a 4th order filter is used for better performance. As the noise shaping order of the ΣΔM is taken to be 3 in the design so the 4th order first stage non-recursive filter is used for better performance and anti-aliasing characteristics. This first stage operates at the rate of oversampling obtained from the oversampling modulator. Input stage of the design is very important due to the fact that it can result in large power dissipation as being working at the highest clock frequency that is why only decimation by 2 stages are used [27].The word-lengths of the two stages are calculated as per the expression:

$$B_{out} = \alpha + B_{in}; \quad (11)$$

Where α is the order of the non-recursive filter and B_{in} is the word-length of the input to the filter. Both these filtering stages are implemented using polyphase decomposition technique.

B. 3rd stage of Filter

The Sinc filter forms the third stage of the decimation filter and is used for further suppression of the quantization noise. This filter is used after the non-recursive filters in order to meet the area constraints of the decimation filter because Sinc filter is an area efficient filter due to the absence of the multipliers and storages.

In the proposed decimation filter the 3rd order Sinc filter performing decimation of 4 is used. If the differential delay D=1 then its transfer function is

$$H_3(z) = \left(\frac{1-z^{-4}}{1-z^{-1}}\right)^3 \quad (12)$$

The polyphase decomposition technique used removes the critical path problem present in the CIC filter architecture and thus increases the speed of operation of the design. Adding to it, only first three registers having small internal word-length operate at higher sampling frequency than others proceeding after down sampler.Thus we can eliminate or share many items implemented through z^{-1} resulting in reduced power consumption.This expression implemented using polyphase decomposition structure is shown in Fig. 5.

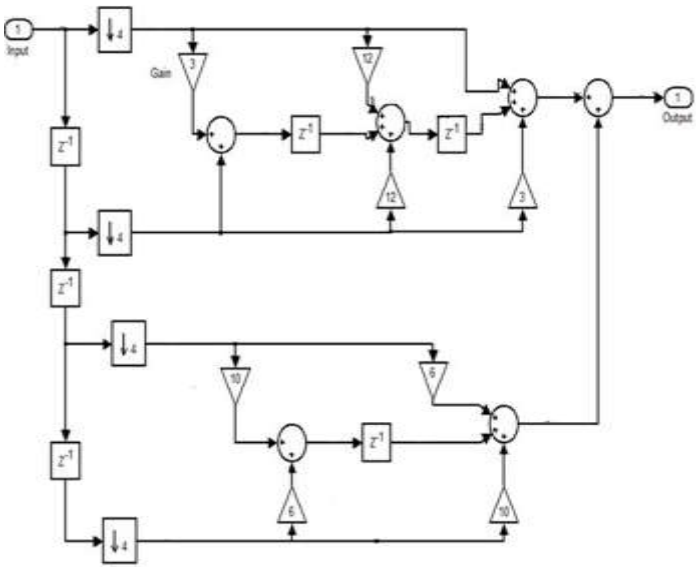

Figure5. H_3 (z) (sub-filter) implementation

C. 4th Stage of Filter (HBFS)

The use of comb filters which are simple in structure have largely reduced the rate of sampling. However, the stopband attenuation achieved is not sufficient to meet the desired application demands. Therefore, a cascaded combination of

two FIR HBFs is used to further increase the stopband attenuation [28]. In this paper, the HBF is implemented with a direct form transposed FIR polyphase decimator structure to reduce power consumption and hardware complexity [5]. The output sampling rate (13MHz) of the 3rd order CIC filter is same as the input sampling rate of the first HBF. Due to down-sampling the output sampling rate of the first half-band FIR filter stage is 6.5MHz. This HBF can be implemented by using a filter of low order whose transition band is relatively wide. Specifications of first HBF are shown in Table 3.

Table 3.specifications of first HBF

Filter type	FIR
Response Type	Low pass
Filter type	Decimator
Stopband attenuation	65dB
Design method	Equiripple

Like 4th stage the 5th stage used in the design is the computationally efficient HBF. Their efficiency lies in the fact that they have approximately half of the coefficients equal to zero implying that large amount of computing power can be saved. Other characteristic of HBFs is that they have equivalent passband and stopband ripples and symmetrical passband and stopband frequencies around Fs/4 of sampling frequency. Due to these advantages they are used as the 4th and 5th stage of the decimation filter design. The 4th stage HBF used in the design is of 6th order. While the 5th stage HBF is of 14th order. The HBFs suppress the initial quantization noise the will relax the requirements for the preceding FIR filter. Both of HBFs use the direct form transposed FIR polyphase decimator structure configuration The HBFs used in the design are obtained using the "filter-builder" option in the MATLAB. The "filter-builder" option helps us to both realize HBF block to be used in SIMULINK and HDL code generation to be used in XILINX.

D. 5th Stage of Filter (LPF)

The final stage of the decimation filter is a 36th order FIR LPF with down-sampling of 2. Like HBFs FIR filter is designed and realized using the "Filter-builder" option in the MATLAB and its HDL code is generated using HDL Coder Toolbox therein. For the HDL code generation CSD format is used to encode the tap coefficients of the HBFs in order to technique in order to increase speed of operation and reduce the computation power.

Table 4. Specifications of FIR filter

Type	**Low pass**
Order	36
Stopband attenuation	60dB
Sampling frequency	3.25MHz
Design method	Equiripple
Phase constraint	Linear
Passband frequency(Normalized)	0.45
Stopband Frequency(Normalized)	0.55

IV. PERFORMANCE EVALUATION

The proposed decimation filter design for Sigma Delta A/D Convertersis targeted for wideband communication with speed and complexity as main design focus along with area conservation.The design setup of the proposed filter is first designed and analyzed using Simulink platform of MatLab and then implemented in Xilinx software using computer with core i7 configuration and windows 10 OS.

A. Implementation

The implementation of the proposed filter is carried out with focus on complexity with power and areafactors addressed as main issues [5, 30]. The decimation filter has been synthesized using Precision Synthesis tool as well in Xilinx and the top view of resulting RTL schematic is shown in Fig. 6. The implementation has been done using:Artix-7 board from FPGA Family; Device: XC7A100T; Package: CSG324, which provides better low power dissipation capabilities, high yield and high density packaging.

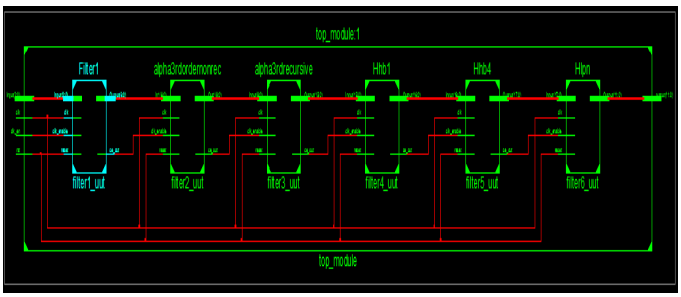

Figure 6. RTL schematic top view of decimation filter

B. Speed and Wordlength Effects

The CIC filter transfer function in the z-plane is given by:

$$H(z)=\left(\frac{1-z^{-DN}}{1-z^{-1}}\right)^{k} \quad (13)$$

Where D is differential delay and is usually 1 or 2.In this paper it is chosen to be 1,k is the filter order and N is decimation factor.The maximum dynamic range growth occurs at the DC frequency (i.e., z = 1), [9]. The maximum dynamic range growth is

$$B_{grow} = (RN)^{k} \quad (14)$$

In bits the growth rate is

$$b_{grow} = \log_2 (B_{grow}) \text{ bits} \quad (15)$$

Knowledge of this value is important when designing a CIC filter, since the need for exact arithmetic. The total internal wordwidth is defined as the sum of the input wordwidth and the maximum dynamic growth requirement, or algebraically:

$$B_{intern} = B_{input} + B_{growth} \quad (16)$$

The delay block (z^{-1}) is implemented as a register whose size is given by the formula:

$$W_i = k \log_2 (RN) + B_{in} \quad (17)$$

Where B_{in} is the number of input bits, W_i is the register size of ith stage. The number of output is also the same as Wi.

If the CIC filter is designed to perform exact arithmetic with this word-width at all levels, no run-time overflow will occur at the output. Fig. 7 shows a 3 stage CIC filter that consists of a 3 stage integrator, a sampling rate reduction by M, and a three-stage comb. Note that all integrators are implemented first, then the decimator, and finally the comb sections. The rearrangement saves a factor M of delay elements in the comb sections. A 3 stage CIC filter with an input wordlength of 8 bits, along with D = 2, N = 32, or DN = 2× 32 = 64, would require an internal wordlength of$W_i = 8 + 3 \log_2 (64) = 26$ bits, to ensure that run-time overflow would not occur. The output wordlength would normally be a value significantly less than W_i, such as 10 bits. This design consideration is used in proposed filter.

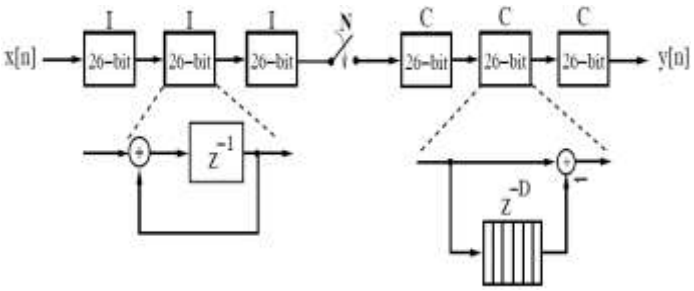

Figure 7. CIC filter with each stage of 26 bit [9]

The word-length effects impact the speed of operation of a multi-rate decimation filter to a great extent. The comparison of increase in word-length of the proposed filter through the different stages is shown in the Table 5.As shown in Table, the final output width of the digital decimation filter is 12 bits for the input of 3 bits. In the decimation filter output, we drop the lower 6 bits of the output of the comb section so that the final output width of the decimation filter becomes a 12-bit word.

Table 5. Wordlength increase through the stages

Word-lengths at the output of each stage		
Stage	*Filter design with recursive input stages*	*Proposed Design*
1st	11	7
2nd	14	10
3rd	17	16
4th	18	17
5th	19	18

C. Area Utilization

The area taken by a device is one of the core factors to decide the efficiency of the design. In order to verify the efficiency of the proposed design a comparison of resource utilization is made in the Fig. 8. It can be seen from the figure that the resource utilization is less in our decimator design as compared to conventional filter architectures popular in literature. So the idea of using non-recursive comb and CIC filter combinationfor design of decimation filter results in optimized area along with less complexity. The design also offers the flexibility that as per requirement of the application one can increase/decrease the number and order of the filtering stages.

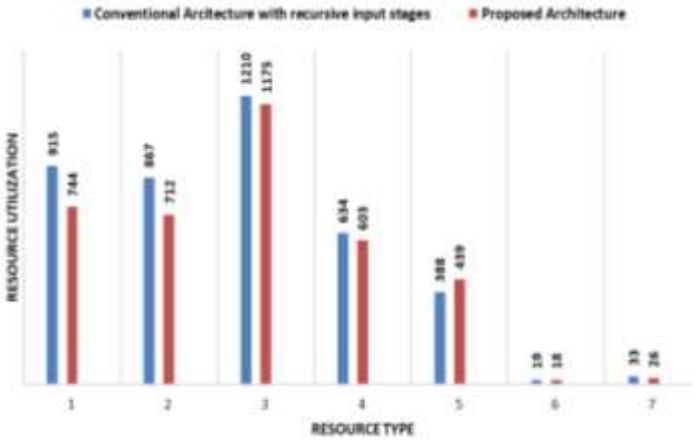

Figure 8. Comparison of used resources in both architectures

V. CONCLUSION

The work in this paper focused on the designing of the low power decimation filter by modifying the already present architectures with different approaches and techniques. The proposed filter has been targeted for wideband applications. The algorithms and the filter structures chosen are hardware realizable in which low power is the most important constraint. The suitable low power techniques are applied in each case to minimize power consumption of the device targeted. The designed filter was targeted for being implemented in FPGA kit. The proposedMulti-rate filter comprises of multiple stages of non-recursive Comb, recursive Comb, HBF and FIR filters. Shift and add operations are used to implement multiplications of CSD-encoded coefficients. HDL synthesis has been preferred choice to implement the functions, including the storage of coefficients and computation, instead of RAM and ROM due to its time-to-market advantage. Experimental results show that use of multi-stage structure, with a proper selection of the decimation factor and filtering stage, ensures efficient

performance of decimation filter. It has been shown that use of non-recursive comb filter results in reduction in word-lengths as achieved by proposed architecture and thereby reduces power consumption and increases speed of operation. Also due to the use of both non-recursive and recursive combs area optimized decimation filter is obtained.

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