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Design of Area Efficient and High Speed Fir Filter Using Distributed Arithmetic with Look up Tables Based On Flip-flop Using Pulsed Latches Technique

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Abstract: In this paper we present design of efficient highly efficient LUT based circuit for the implementation fir filter using Distributed arithmetic algorithm. It is a multiplier less fir filter designed and design based on Distributed arithmetic algorithm. The based technique consists of Look Up Table (LUT), shift registers and scaling accumulator. In this paper, the shift registers can be designed by using flip flop based on pulsed latch technique. The proposed architecture of fir filter is designed and synthesized using Xilinx software and its provides an efficient area-time-power implantation which improves latency and less area- delay complexity through pulsed latch technique when compared with existing structure for FIR filter.

Keywords: Distributed Arithmetic (DA), fir filter, flip-flop, look up table (LUT), latch, and Shift register.

I. INTRODUCTION

Finite impulse response (FIR) digital filters are extensively used due to their key role in various digital signals processing (DSP) application. Along with the advancement in very large scale integration(VLSI)technology as the DSP has become increasingly popular over the years, the high speed realization of fir filters with area efficient has become more demanding [7][8].Since the complexity of implementation grows with the filter order and the precision of computation, real-time realization of these filters with desires level of accuracy is challenging task. Several attempts have, therefore, been made to develop dedicated and reconfigurable architecture for realization of FIR filter in field programmable gate array (FPGA) platforms. Systolic designs represent an attractive architectural paradigm for efficient hardware implementation of computation- intensive DSP applications, being supported by the features like simplicity, regularity and modularity of structure. A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in much application, such us digital filters, communion receivers and image processing. As the word length of the shift register increases, the area and power consumption of the shifter register become important design considerations. The architecture of a shift register is quite simple. An N-input shift register is composed of series connected N data flip-flops.the speed flip-flop is less important than the area and power consumption because there is no circuit between flip-flop sin the shift register[1][2].

II. CONVENTIONAL MULTIPLIER AND ACCUMULATOR BASED FIR FILTER

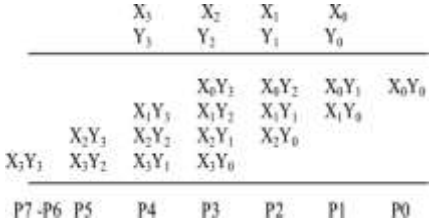
However, the multiplier in these structures needed large portion of chip area, consequently enforce limitation on the maximum possible number processing elements (PEs) that can be accommodated and the highest order of the filter that can realized[8][9] .

Array multiplier

In this method array multiplier is used to form multiplier and accumulator based fir filter. A array multiplier can be divided into three parts i) partial product generation ii) partial product addition and iii) final addition.

But these multipliers consume more Area and delay.

Fig.1 Array Multiplier Archeitecture



Area and delay has become a critical concern in today's VLSI system design. Hence the designers are needed to concentrate efficient multipliers for the design

of efficient FIR filter in DSP systems [6] [7]. The architecture of FIR filter using array multiplier inFig.2.

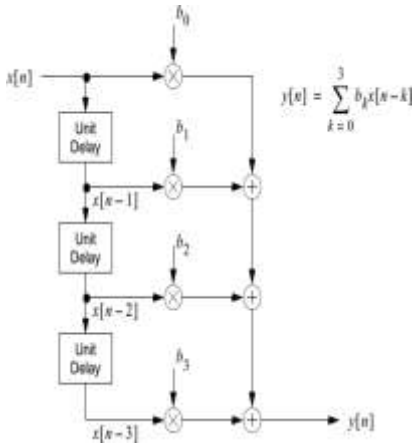


Fig.2. Array multiplier architecture

III. PROPOSED FIR FILTER ACHITECURE USING DISTRIBUTED ARITHMETICWITHLOOKUPTABLES BASED ONFLIPFLOP

A. shift register using flip-flop:

The multiplier less distributed arithmetic (DA)-based technique has gained substantial popularity, in recent years, for its high-throughput processing capability and increased regularity which results in cost- effective and area-time efficient computing structures. The main operations required for DA-based computation of inner product are a sequence of lookup table (LUT) accesses followed by shift- accumulation operations of the LUT output. DA-based computation is well suited for FPGA realization, because the LUT as well as the shift-add operations, can be efficiently mapped to the LUT-based FPGA logic structures.

In FIR filtering, one of the convolving sequences is derived from the input samples while the other sequence is derived from the fixed impulse response coefficients of the filter. This behavior of the FIR filter makes it possible to use DA-based technique for memory-based realization. It yields faster output compared with the multiplier-accumulator-based designs because it stores the pre computed partial results in the memory elements, which can be read out and accumulated to obtain the desired result[6]-[9].

The memory requirement of DA- based implementation for FIR filters, however, increases exponentially with the filter order.

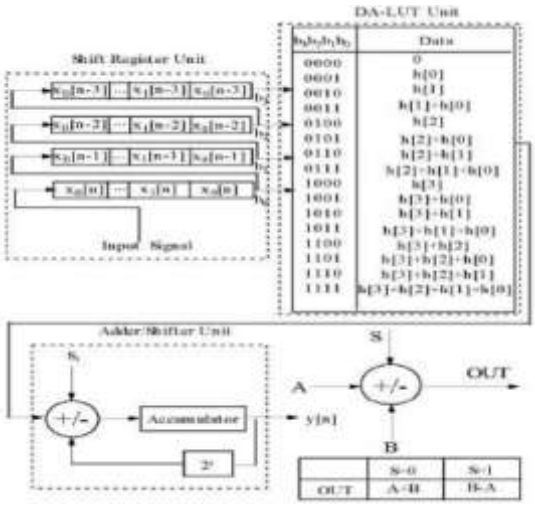


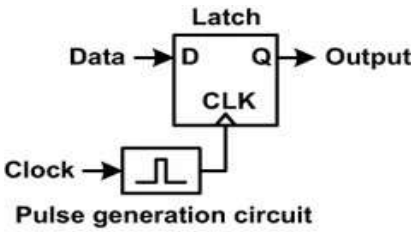
Fig.3.FIR filter DA_LUT with normal FF

B. shift registers using proposed flip- flop:

The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. Butthepulsedlatchcannotbeusedin a shift register due to the timing problem between pulsed latches. In this paper represent a area efficient and high speed shift register using pulsed latch The shift register solves the timing problem using multiple non- overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches[3][4].

All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, they are a and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.

Fig.4.Pulse D latch.



The output signal of the first latch(Q1) changes correctly because the inputs signal of the first latch(IN) is constant during the clock pulse width (T pulse). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

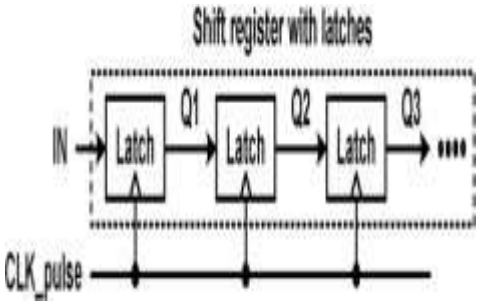


Fig.5 Shift register with Latches

C. *Delayed pulsed clock signal*

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 5. The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 3(b) the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width , but the input signals of the second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1andQ2)after the clock pulse[2]-[5].

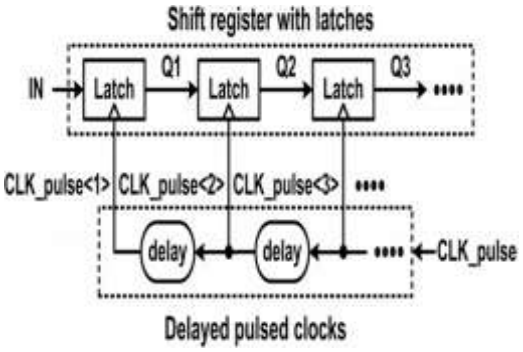


Fig.6.Shift register withlatchesand delayed pulsed clock signals

D. *proposed shift register*

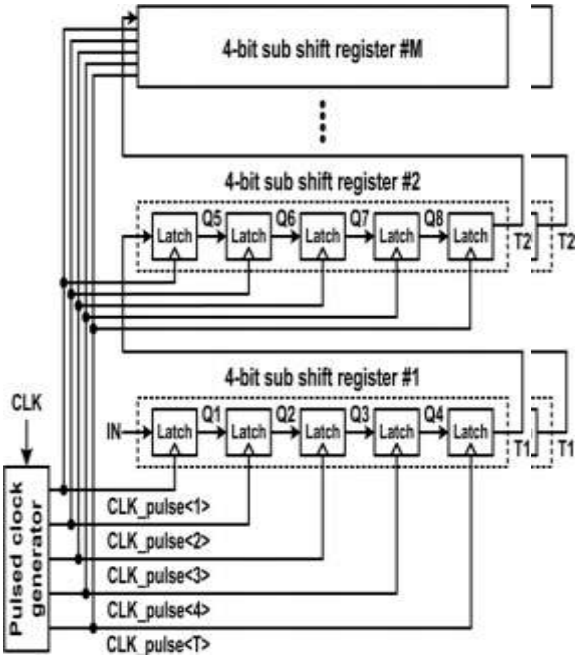


Fig.7.Block diagram of proposed shift register

Finally we have to deign are a efficient and high speed digital fir filter using distributed arithmetic algorithm with look up table. In this design consist of combine different circuit such as pulsed latch, shift register;adder/subtractandaccumulatorblock.Blockdiag ramproposedfirfilterusing shift register by using pulsed latch technique is given below [6].

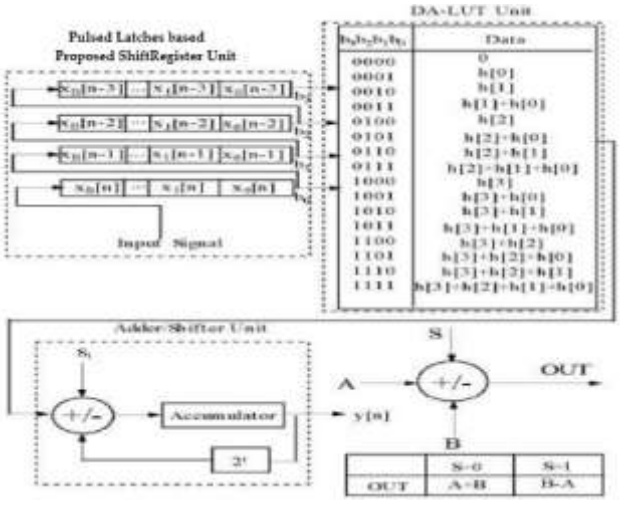


Fig.8 Block Diagram of proposed work

IV. SIMULATION OUTPUT AND COMPARISON RESULT

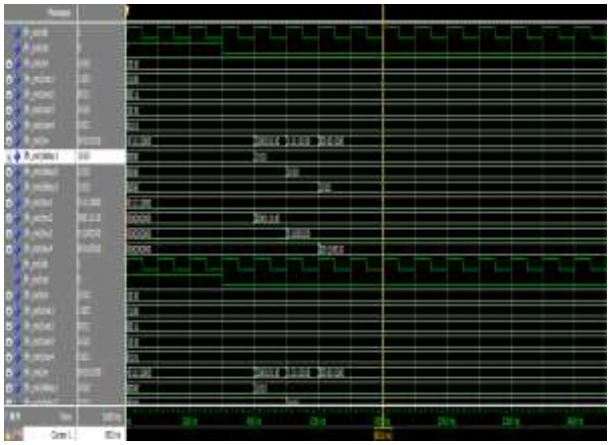


Fig.9.simulation output of Digital Fir filterusingarraymultiplier

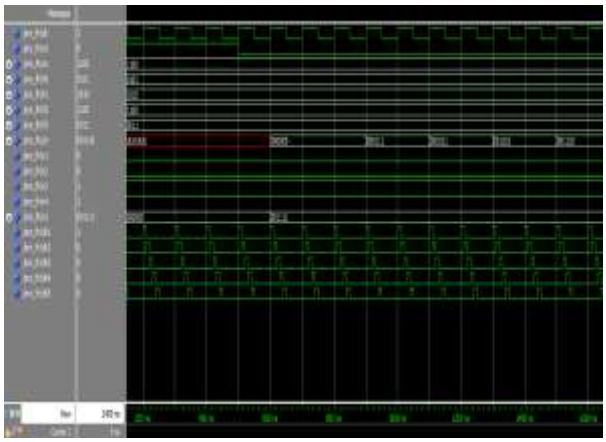


Fig.10.Simulation output of Digital FIR filter using proposed shift register

Table-1. Comparison of Area, Delay, and Power between Three Different Methods of Fir Filter Design

Methodology	*LUT*	*DELAY (ns)*	*POWER (mW)*
Fir filter Using Array multiplier	*146*	*14.730*	*118*
Fir filter Using Normal FF	*144*	*9.138*	*228*
Fir filter using proposedFF	*4*	*4.671*	*117*

V. CONCULSION

In this paper, we have to convert complicated multiplication and accumulation operation into the shifting and adding operation when the Distributed arithmetic algorithm is directly applied to realize the digital fir filter. The shift register are very important role in data storing and data shifting operation in digital fir filter. The shift register can be design using pulse d latch technique. In this method, hardware complexity will be reduced. Finally, the digital fir filter has been simulated and synthesized in Xilinx software and also analysis area, power and delay of digital fir filter.

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